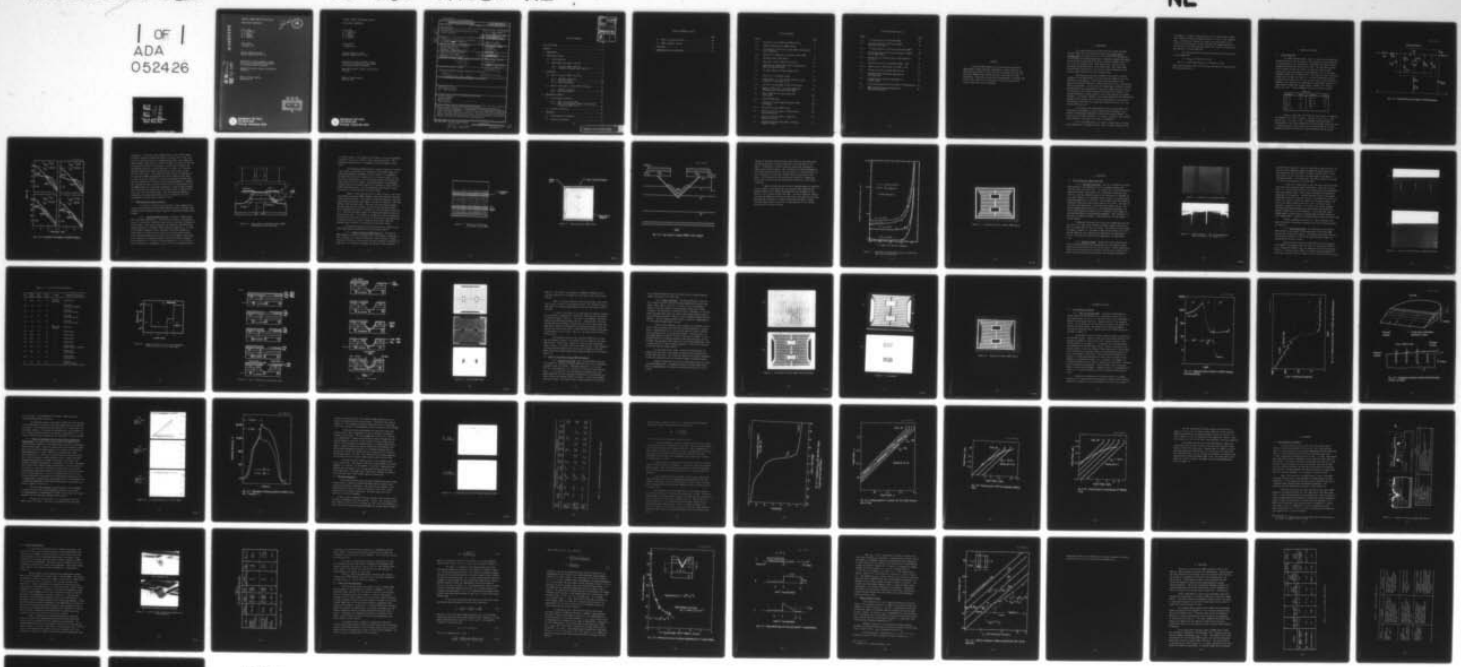
AD-A052 426 WESTINGHOUSE RESEARCH AND DEVELOPMENT CENTER PITTSBU--ETC F/G 9/1
VERTICAL CHANNEL METAL-OXIDE-SILICON FIELD EFFECT TRANSISTOR.(U)
NOV 76 T M HENG, R A WICHSTROM, J G OAKES N00014-74-C-0012

UNCLASSIFIED 76-9G7-VMOST-R2 NL

1 OF 1
ADA
052426



END
DATE
FILMED
5-78
DDC

VERTICAL CHANNEL METAL-OXIDE-SILICON FIELD EFFECT TRANSISTOR

T.M.S. Heng
R. A. Wickstrom
J. G. Oakes
D. A. Tremere
E. T. Watkins

FINAL REPORT
1 November 1976

Contract N00014-74-C-0012
Contract Authority NR 251-013

Office of Naval Research
Washington, DC

Westinghouse R&D Center
1310 Beulah Road
Pittsburgh, Pennsylvania 15235

VERTICAL CHANNEL METAL-OXIDE-SILICON

FIELD EFFECT TRANSISTOR

T.M.S. Heng
R. A. Wickstrom
J. G. Oakes
D. A. Tremere
E. T. Watkins

FINAL REPORT
1 November 1976

Contract N00014-74-C-0012
Contract Authority NR 251-013

Office of Naval Research
Washington, DC

Westinghouse R&D Center
1310 Beulah Road
Pittsburgh. Pennsylvania 15235

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NR 251-013 FTR
2. GOVT ACCESSION NO.:
3. RECIPIENT'S CATALOG NUMBER:

4. TITLE (and Subtitle): Vertical Channel Metal-Oxide-Silicon Field Effect Transistor

5. TYPE OF REPORT & PERIOD COVERED: Final - Thru November 1, 1976

6. PERFORMING ORG. REPORT NUMBER: 76-9G7-VMOST-R2

7. AUTHOR(s): T.M.S. Heng, R.A. Wickstrom, J.G. Oakes, D.A. Tremere, E.T. Watkins

8. CONTRACT OR GRANT NUMBER(s): N00014-74-C-0012

9. PERFORMING ORGANIZATION NAME AND ADDRESS:
Westinghouse Electric Corporation
Research Laboratories
Pittsburgh, Pennsylvania 15235

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS:
PE 62762N
RF 54-581-001
NR 251-013

11. CONTROLLING OFFICE NAME AND ADDRESS:
Office of Naval Research
Department of the Navy, Code 427
Arlington, Virginia 22217

12. REPORT DATE: 1 November 1976

13. NUMBER OF PAGES: 69

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 69p.

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

F54581

Final rpt. Oct 75 - Sep 76,

RF54581001

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES
ONR Scientific Officer
Tel: (202) 692-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
Silicon Transistor
Vertical Channel
MOS Transistor
Power Transistor
(60 deg.)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Three new VMOST geometries were designed and studied for improvements of power-frequency performances. Output powers up to 10W have been obtained at 1 GHz, with associated gains of 5 dB, from top-source VMOST devices fabricated using a low angle (60°) gate evaporation. The sources of gate oxide contamination in V-groove type devices and a model for the variation of turn-on resistance with V-groove depth were also investigated.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

376 625

Enclosure (2)

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

LIST OF CAPTIONS

LIST OF CAPTIONS (cont'd.)

ABSTRACT

Three new VMOST geometries were designed and studied for improvements of power-frequency performances. Output powers up to 10W have been obtained at 1 GHz, with associated gains of 5 dB, from top-source VMOST devices fabricated using a low angle (60°) gate evaporation. The sources of gate oxide contamination in V-groove type devices and a model for the variation of turn-on resistance with V-groove depth were also investigated.

1. INTRODUCTION

This report describes the work which was carried out under Contract N00014-74-C-0012 during the period from October 1975 to September 1976. The objective of this final phase of the program was to investigate and develop techniques for improving the gain performance of the silicon vertical MOS field effect transistor (VMOST) device in the 2 to 4 GHz frequency band. More specifically, the device must be capable of delivering up to 5W of output power, have linear amplitude and phase characteristics, and a noise figure comparable to the silicon bipolar transistor at this frequency band.

From optimized transistor parameters predicted by computer simulation of the VMOST device, two new transistor geometries were considered for investigation. These required the development of new epitaxial growth and anisotropic etching technologies which, unfortunately, lead to new problems. In the course of studying these problems, a better understanding of the requirements of high power VMOST design was derived. The solutions to the etching problem also provided some insights to the complex dependence of surface stability and surface mobility on chemical treatment. The results, therefore, have wider implications than the present program, and may perhaps aid in a better understanding of the problems experienced by other vertical channel MOS transistor devices, e.g., the V-groove MOS transistor.

In retrospect, the investigation of two new geometries, each requiring the development of fairly sophisticated technologies, was perhaps too demanding and beyond the scope of the present program. As such, the work remains incomplete. The results obtained so far, however, should provide a sound basis for future investigations.

The silicon VMOST device is a viable product today for linear power amplication at frequencies below 2 GHz. A single transistor cell,

for example, is capable of delivering up to 5W of linear Class A power with a reasonably high power added efficiency (> 25%) in this frequency range. This equals or exceeds the single cell output power of the silicon bipolar transistor, and for many UHF band communication applications the vertical MOS transistor should offer superior linearity and more attractive circuit properties.

The milestones which were achieved during the last three years of the program were:

(i) an f_{max} of greater than 4 GHz

and (ii) a power-gain product of 60 dB-watt at 1 GHz.

These are the highest values that have been achieved for a power silicon MOS transistor to date.

2. VMOST DEVICE DESIGN

2.1 Device Modelling

The VMOST computer model, Figure 2.1, which was developed and refined during the first two phases of the program was used extensively at the beginning of this study period to determine the optimum design parameters for high gain operation at S-band. Of particular interest in the simulations were the roles of the parasitic gate-to-drain capacitance, C_{GD}, and extrinsic source inductance, L_{SP}, on the gain-frequency behavior of the VMOST device. The results of four interesting design cases are shown in Figure 2.2. In these simulations the gate periphery was assumed to be 1.75 cm, and the values of the other device parameters were obtained from representative experimental results of a large number of VMOST runs (Annual Report, November 1975, Contract N00014-74-C-0012). These parameters are given in Table 2.1 below.

TABLE 2.1

Parameter	Value	Parameter	Value
C_{GS}, pF	5.8	R_{SP}, Ω	0.05
R_G, Ω	1	R_{GP}, Ω	0.5
C_{DS}, pF	9.4	L_{GP}, nH	0.2
R_D, Ω	60	R_{DP}, Ω	0.1
C_{GN^+}, pF	1.2		

Figure 2.2 shows that the unilateral gain curves, as expected, are dependent only on the C_{GD} value. For C_{GD} = 1.5 pF, f_{max} = 8 GHz, and for C_{GD} = 1 pF, f_{max} = 9 GHz. The maximum stable gain (MSG) is affected both by C_{GD}, which determines the overall amount of MSG (as seen by comparing curves A and C) and by L_{SP}, which peaks MSG at the same frequency at which the stability K factor peaked for various source

Dwg. 6415A24

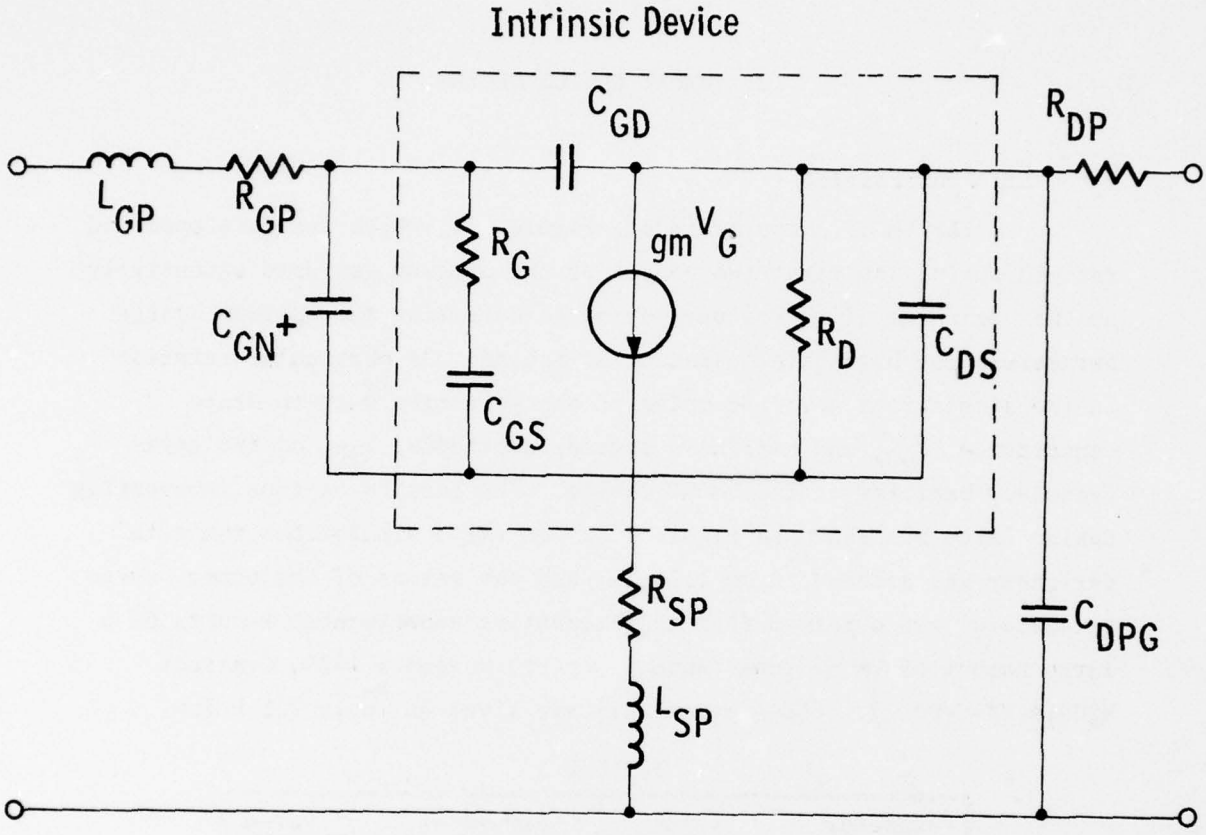


Fig. 2.1 – Equivalent circuit model for VMOST devices

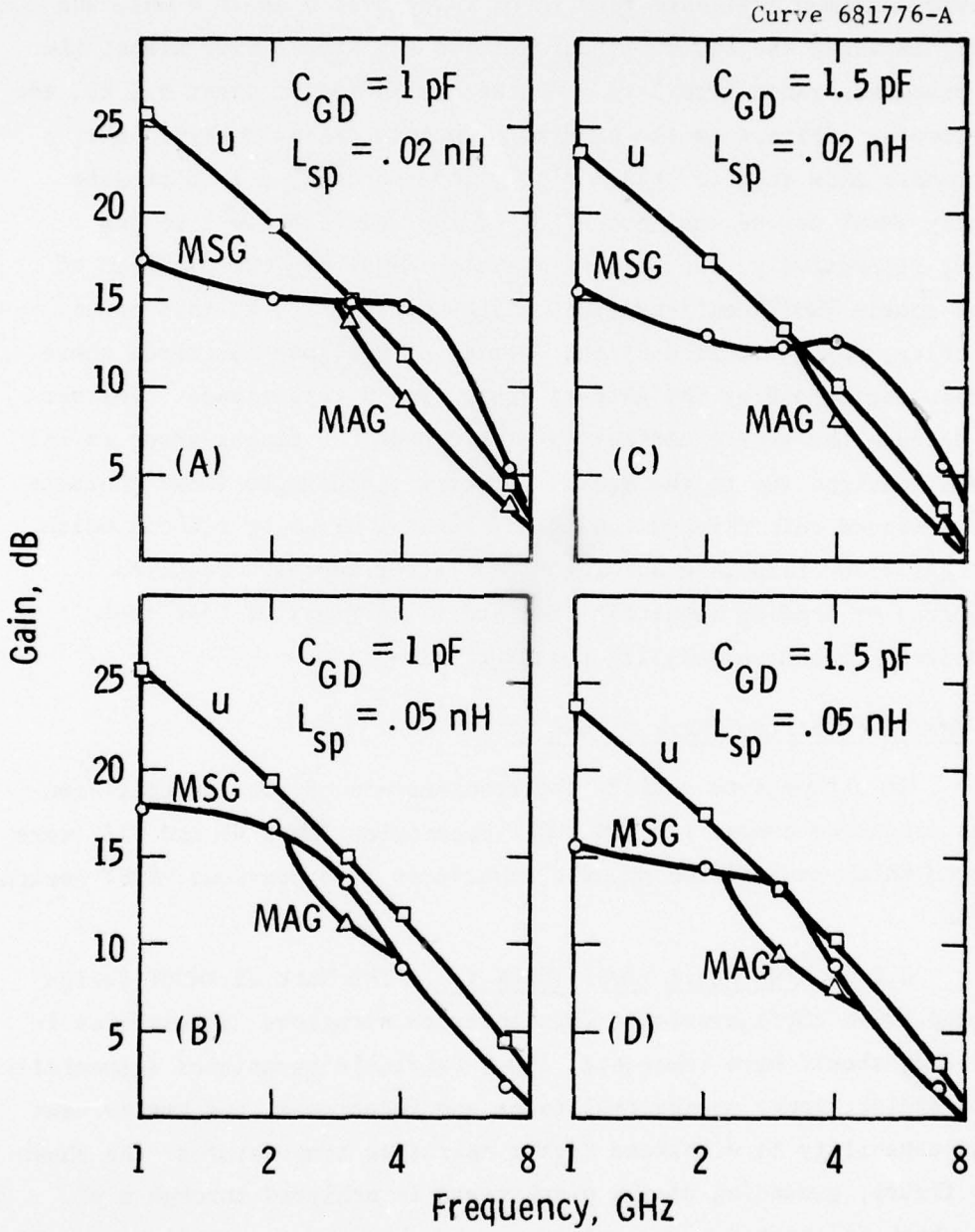


Fig. 2.2 — Computer simulations of VMOST designs

inductances. Of the four cases considered here, case A, which shows the device maximum available gain (MAG) to be over 9 dB at 4 GHz, and curve B, in which the device is unconditionally stable over almost the whole frequency range from 2 to 4 GHz with a MAG of at least 8.5 dB, are of particular interest to the program. In both cases, however, the requirements show that to obtain high gain at S-band, a 1.75 cm gate periphery VMOST device must have C_{GD} and L_{SP} values below 1 pF and 0.05 nH, respectively. Both limiting values indicate the problems of the top-source VMOST configurations which were studied to this point. In practice, C_{GD} is limited by the overlap of the gate electrode above the drain region and by the gate-to-drain trough capacitance. Furthermore, because the source contacts are on top of the finger mesas in all the VMOST designs (up to the Mark V geometry), access to these contacts can be achieved only through the use of bonding wires or ribbons which raise L_{SP}, or by flip-chip bonding. The latter approach requires a high degree of bonding sophistication and is marginal at best from reproducibility and reliability points of view.

2.2 VMOST Geometries (Mark VI and VII)

In attempts to satisfy the requirements of the computer simulations discussed above, two new VMOST geometries (Mark VI and VII) were developed which represented drastic departures from previous VMOST design concepts.

2.2.1 Top-Drain VMOST (Mark VI). The Mark VI VMOST design has a top drain configuration. This inverted structure, illustrated in Figure 2.3, should have inherently lower extrinsic parasitics (especially gate-to-drain), lower source resistance and inductance, and better heat sinking capability to withstand higher operating temperatures. As shown in the figure, grounding of the p-substrate is achieved through a p^+ column which is shorted to the n^+ source by the source metallization. The p^+ grounding column could either run the entire length of the finger or be truncated into grounding islands similar to the Mark V geometry. The resistance of a 4 μm wide, 10 μm high column of 5×10^{-3} Ω-cm resistivity p^+ material, corresponding to 2.5×10^{19} cm^{-3} p concentration, is

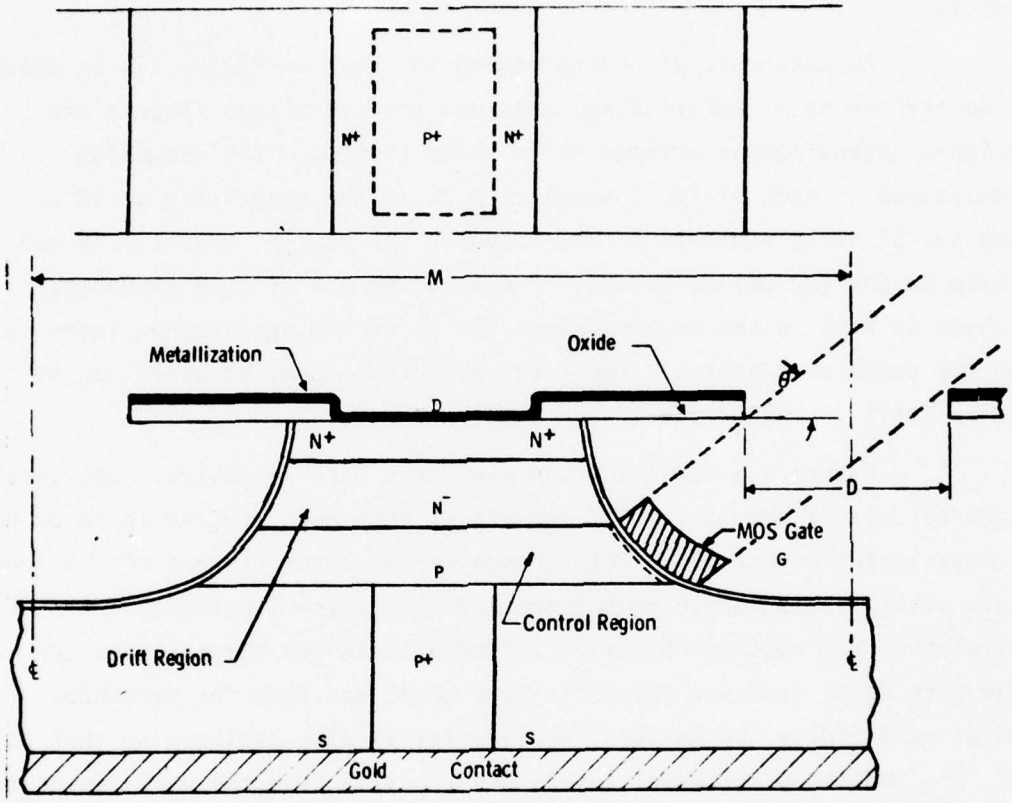


Figure 2.3 Cross-section of Substrate Source VMOST Configuration (post grounding)

$(1.25 \times 10^{-2}/\ell)$ohms. If the length of the column is 50 μm, the grounding resistance is only 2.5Ω, which is much lower than required. This grounding scheme requires an alignment of the mesa fingers to the p^+ posts.

An alternate grounding scheme is shown in Figure 2.4 in which wide stripes of p^+ material are used and the transistor fingers are aligned approximately orthogonal to these stripes. The grounding resistance of each strip is again only 2Ω if the mesa width is 10 μm and the p^+ strip width is 25 μm, assuming the same p^+ resistivity and strip height (10 μm) as before. One disadvantage of this grounding scheme is that in the regions where the p^+ grounding is done, there is no MOS transistor action. The total grounding area, however, can be quite small (< 10% of the active transistor area).

Figure 2.5 shows the top view of a Mark VI device. The isolation notches of previous VMOST geometries have been removed in favor of a mesa isolation barrier. This change is important because of the lower gate metallization angle requirement of the device (typically < 60° with respect to the vertical plane). The mesa isolation barrier isolates the gate metal from the parasitic gate metal and from the periphery metal surrounding the device. The barrier is also designed so that the n^+, n^-, and the p epitaxial layers are isolated from the main device to minimize parasitics. This feature is accomplished simply by narrowing the protective oxide mask at the ends of the barrier so that during the silicon etch step the silicon is undercut sufficiently under the narrowed oxide to result in isolation of the epitaxial layers.

The gate bonding mesas and drain contacts are similar to the other VMOST geometries described in the last Annual Report.

2.2.2 V-Groove Top-Source VMOST (Mark VII). The Mark VII VMOST geometry is based on a modification of the V-groove technology, as shown in Figure 2.6. Unlike conventional V-groove devices, the gate-source metal overlap is minimized by the oxide overhangs in the Mark VII transistor. As originally envisaged, the design has the attractive

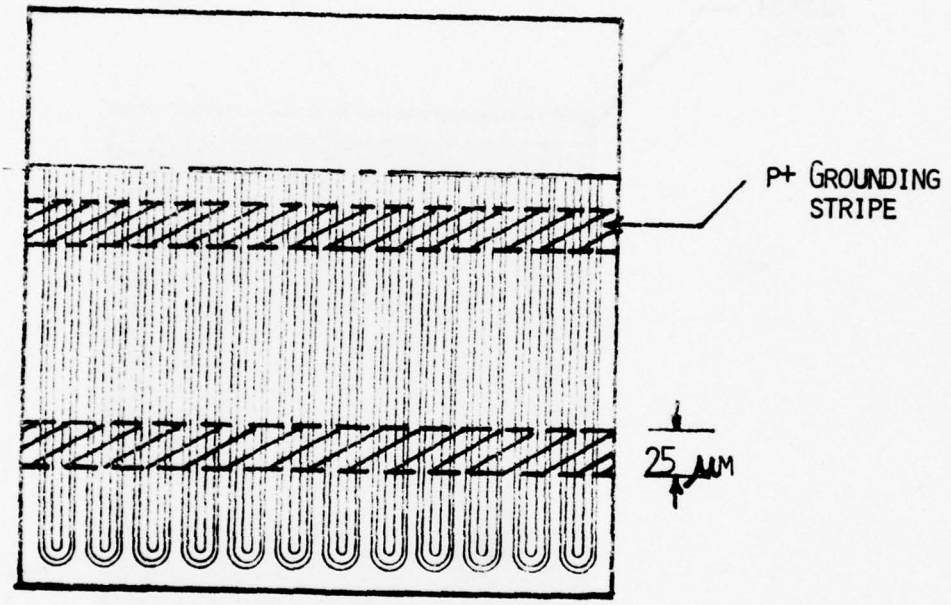


Figure 2.4 Design of p^+ Ground Bus
of Substrate Source VMOST

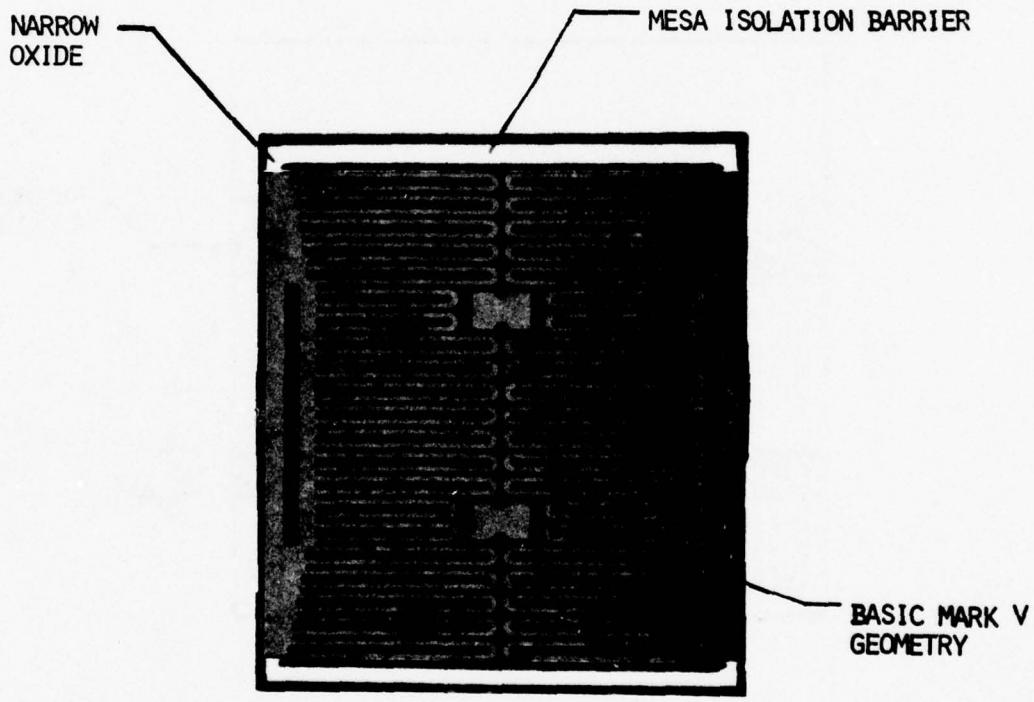


Figure 2.5 Substrate Source VMOST Device

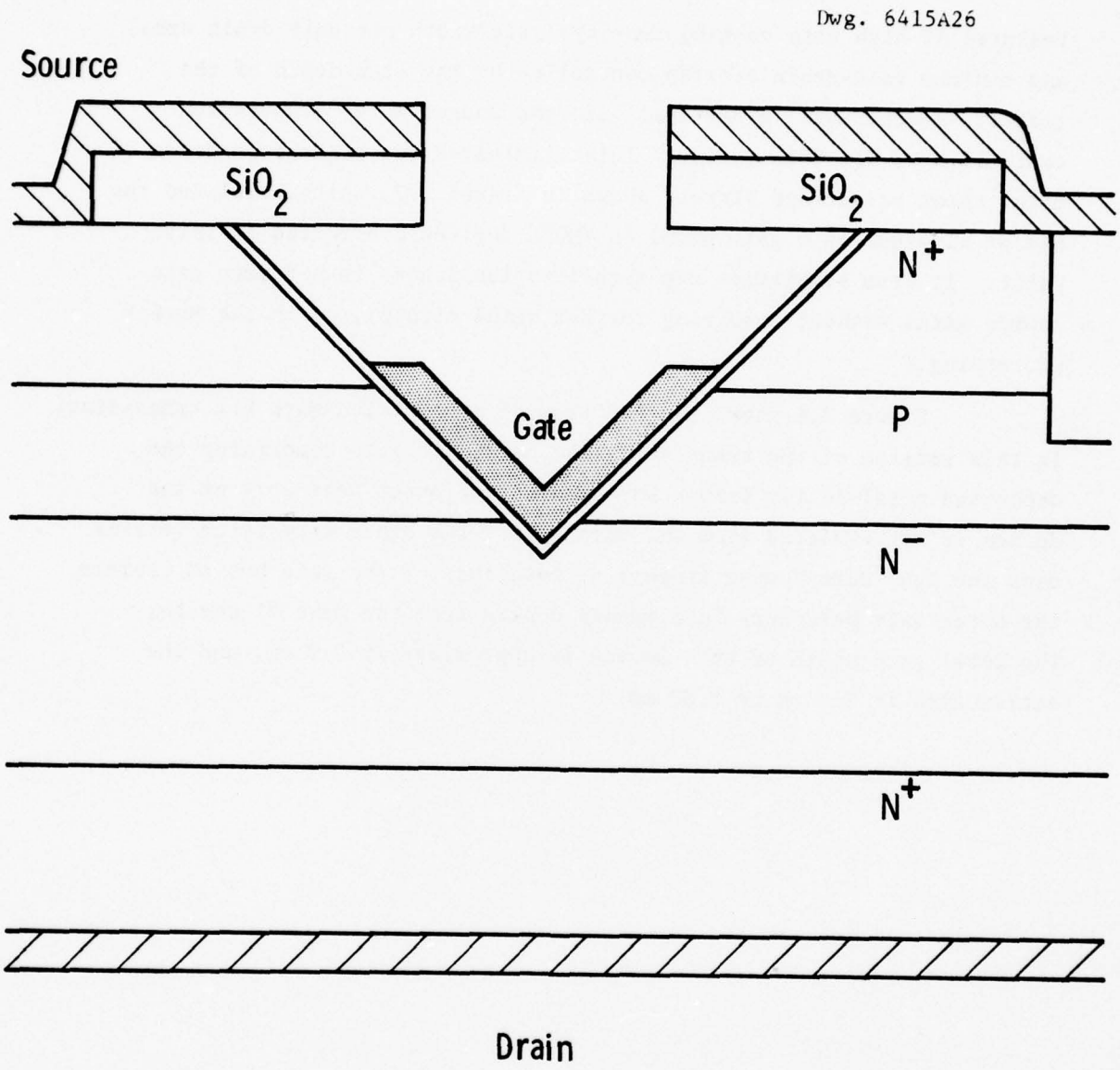


Fig. 2.6 — Top-source V-groove VMOST cross-section

features of high gate packing density (gate width per unit drain area) and minimum gate-drain overlap controlled by the etch depth of the groove. Furthermore, a vertical gate and source metal evaporation could be used for this device. This eliminates the angle dependence of metal sheet resistance effect, shown in Figure 2.7, which precluded the use of aluminum as a gate metal in VMOST devices fabricated to this point. It also simplifies the metallization scheme to a common gate-source metal without requiring further metal etching, as in the Mark V processing.

Figure 2.8 shows the top view of a completed Mark VII transistor. In this version of the transistor, the parasitic gate comprising the deposited metal in the trough surrounding the outer periphery of the device is not isolated from the main gate. The other transistor version uses the two "dummy" mesa fingers at both ends of the gate bus to isolate the outer gate periphery in a manner copied from the Mark VI design. The total gate width of this device is approximately 0.9 cm, and the active area is 0.3 mm by 0.39 mm.

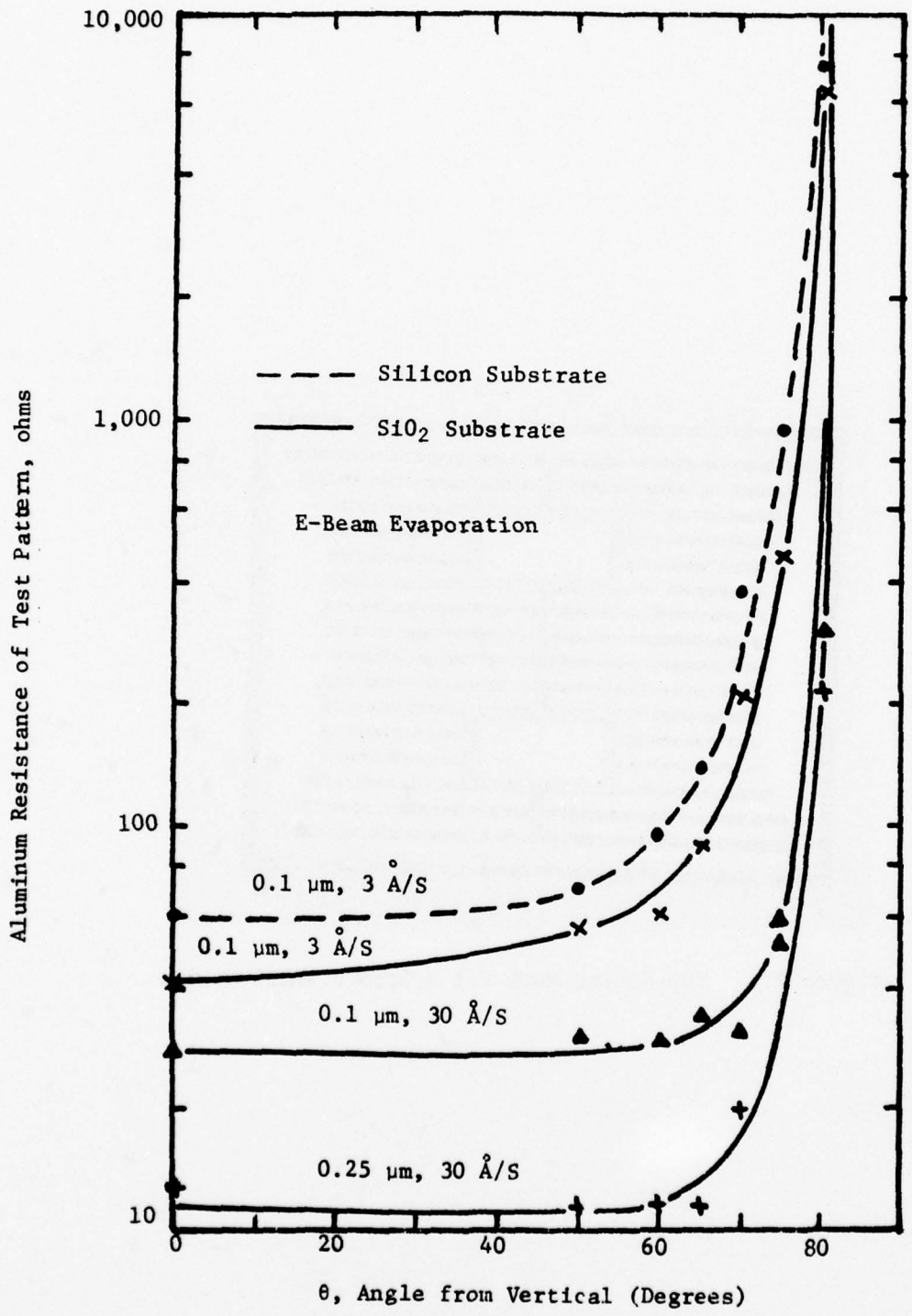


Figure 2.7 Dependence of Aluminum Resistance on Evaporation Angle and Deposition Rate

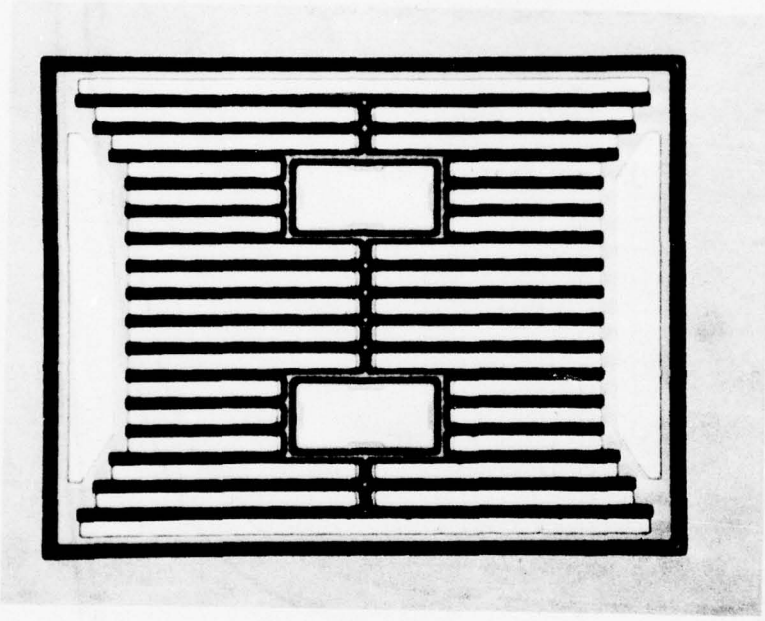


Figure 2.8 Top-Source Mark VII V-Groove VMOST Device

3. FABRICATION

3.1 Mark VI Top-Drain VMOST Processing

3.1.1 Substrate Processing. The key to the Mark VI inverted VMOST geometry is the formation of the p^+ grounding regions with vertical walls of at least 10 μm. To achieve this, a starting substrate material of 0.008 Ω-cm As-doped, <110> orientation silicon was used. Initially, SiO_2 was thermally grown on the substrate to a thickness of 1 μm, and a pattern of p^+ grounding strips (Figure 3.1) was delineated photolithographically on the oxide. Stripe windows were then formed by chemically etching the exposed oxide down to the silicon. The width of the oxide strip opening was 3 μm and the strip length 0.94 mm. The spacing between stripes was 50 μm. In delineating the patterns, the strips were aligned at an angle of 54.7° (clockwise) with respect to the substrate wafer flat during photolithography. This orientation is necessary to produce a minimum of undercutting of the <111> planes during etching.

Preferential etching of the silicon was accomplished with the use of a 44 wt % KOH and H_2O etchant to produce a higher etch rate on the <110> planes than on the <111> planes. The results of this etching are shown in Figure 3.2. The depth of the vertical grooves was 42 μm, and the width was 4 μm, indicating an undercutting of approximately 0.5 μm. The wafer was etched at room temperature for approximately 24 hr.

3.1.2 Epitaxial Growth. Backfilling of the etched grooves with p^+ (B-doped) material was accomplished on a CVD (chemical vapor deposition) epitaxial H_2-$SiCl_4$-HCl reactor system. The HCl effectively etches the silicon which tries to grow on the top <110> surface of the wafer, resulting in zero net deposition, while allowing preferential

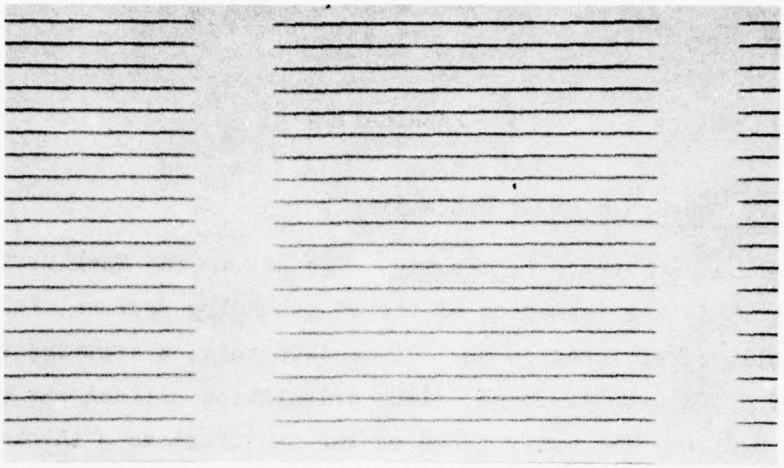


Figure 3.1 Pattern of p^+ Grounding Stripes

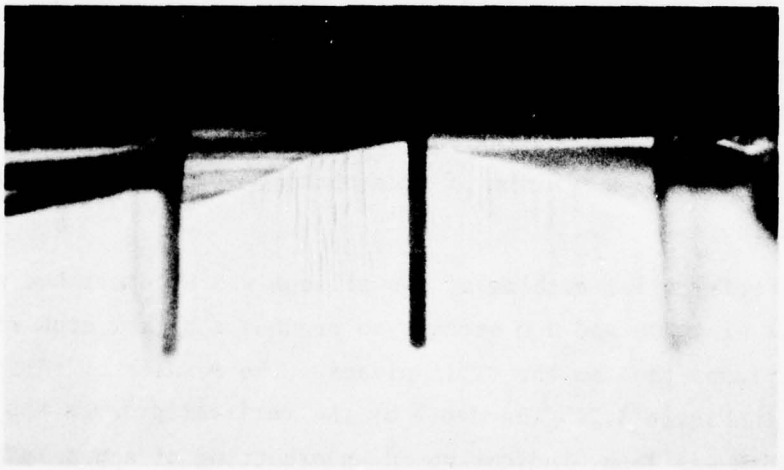


Figure 3.2 Etched Grooves in <110> Silicon Substrate, Width of Grooves, 4 μm; Height 42 μm.

net growth in the grooves. Thus, too little HCl allows the top of the grooves to fill before the bottom is completely filled and leaves a void beneath the silicon surface, as shown in Figure 3.3(a). On the other hand, too much HCl causes the upper edges of the groove to etch back and widen. In extreme cases, the whole surface of the wafer is etched, thereby reducing the groove depth.

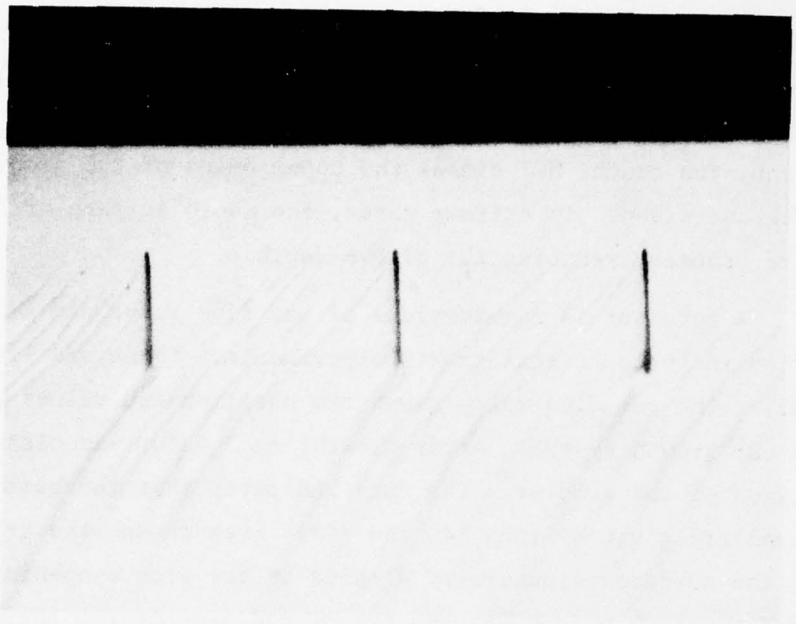
A total of 13 combinations of gas flow rates and growth times were tried in the epitaxial growth experiments. These are listed in Table 3.1. The gas flow rates given are uncalibrated values applicable only to our growth system. After growth, each wafer was cleaned for examination of the grooves. The data indicates that the best growth conditions are given by runs #40 and #49. Even though the grooves are filled, the surface is generally dimpled at the groove openings, and thus is not smooth enough to grow the p- and n-epitaxial layers required to complete the wafer. To eliminate the surface roughness, the wafers were Syton polished back lightly after each backfilling growth to remove up to 10 μm of material. This still left a deep enough groove to ensure contact to ground after substrate thinning of the finished wafer. A photo of a polished wafer is shown in Figure 3.3(b).

Finally, epitaxial layers of p, n^-, and n^+ materials were grown on the back-filled wafer according to the ideal profile sketched in Figure 3.4.

3.1.3 Device Fabrication. The fabrication of the Mark VI VMOST device is very similar to the fabrication of the other VMOST devices, and in some senses simpler. The detailed processing steps are illustrated in Figure 3.5, for the case where the drain fingers are aligned at 90° to the p^+ strips.

The first step in the device fabrication is the delineation of the VMOST oxide geometry, Mask A, Figure 3.6, after which 1000Å of Si_3N_4, followed by 1600Å of SiO_2, are deposited over the oxide pattern, Step (2). A second pattern, Mask B, is defined photolithographically on the SiO_2, and the latter is etched to form an etch mask for the Si_3N_4,

(a)



(b)

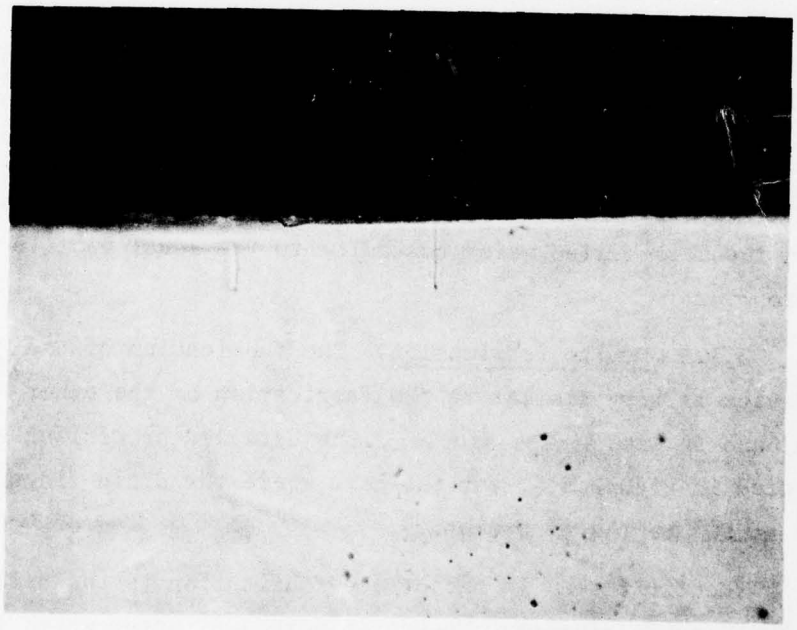


Figure 3.3 Side View (cleaved edge) of Back-Filled Slots

TABLE 3.1 Slot Backfilling Experiments

Run	$SiCl_4$ Rate	HCl Rate	Time (min)	Dopant	Comments/Description
35	150	62	45	Low conc. phosphene	Bottom open
36	75	53	45	"	Top open Growth not complete
38	75	56	90	"	Top open SiO_2 left on top
39	75	50	90	"	Top open SiO_2 left on top
40	75	40	90	"	Top open SiO_2 left on top
41	75	40	40	High conc. diborane	Unfilled
42	150	40	40	"	Bottom open
43	150	50	40	"	Bottom open
44	150	50	40	"	Bottom open
45	150	55	40	"	Bottom open
46	150	60	40	"	Bottom open Better than 45, however
47	150	65	40	"	Bottom open Poor filling
48	75	75	40	"	Bottom open Contradicts 41
49	75	40	80	"	Top open Possibly useful

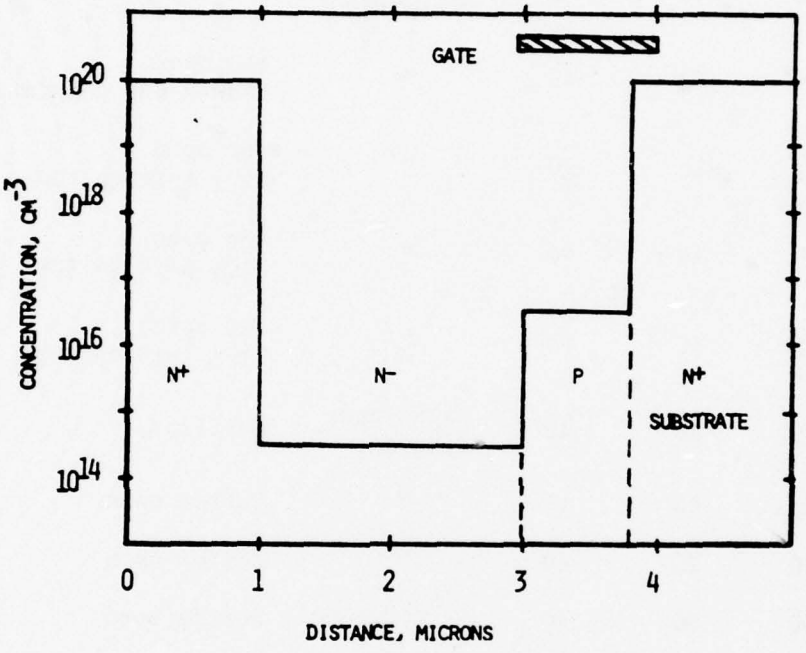


Figure 3.4 Impurity Profile for 1.76 cm Gate Periphery Substrate Source Inverted S-Band VMOST

Step 2

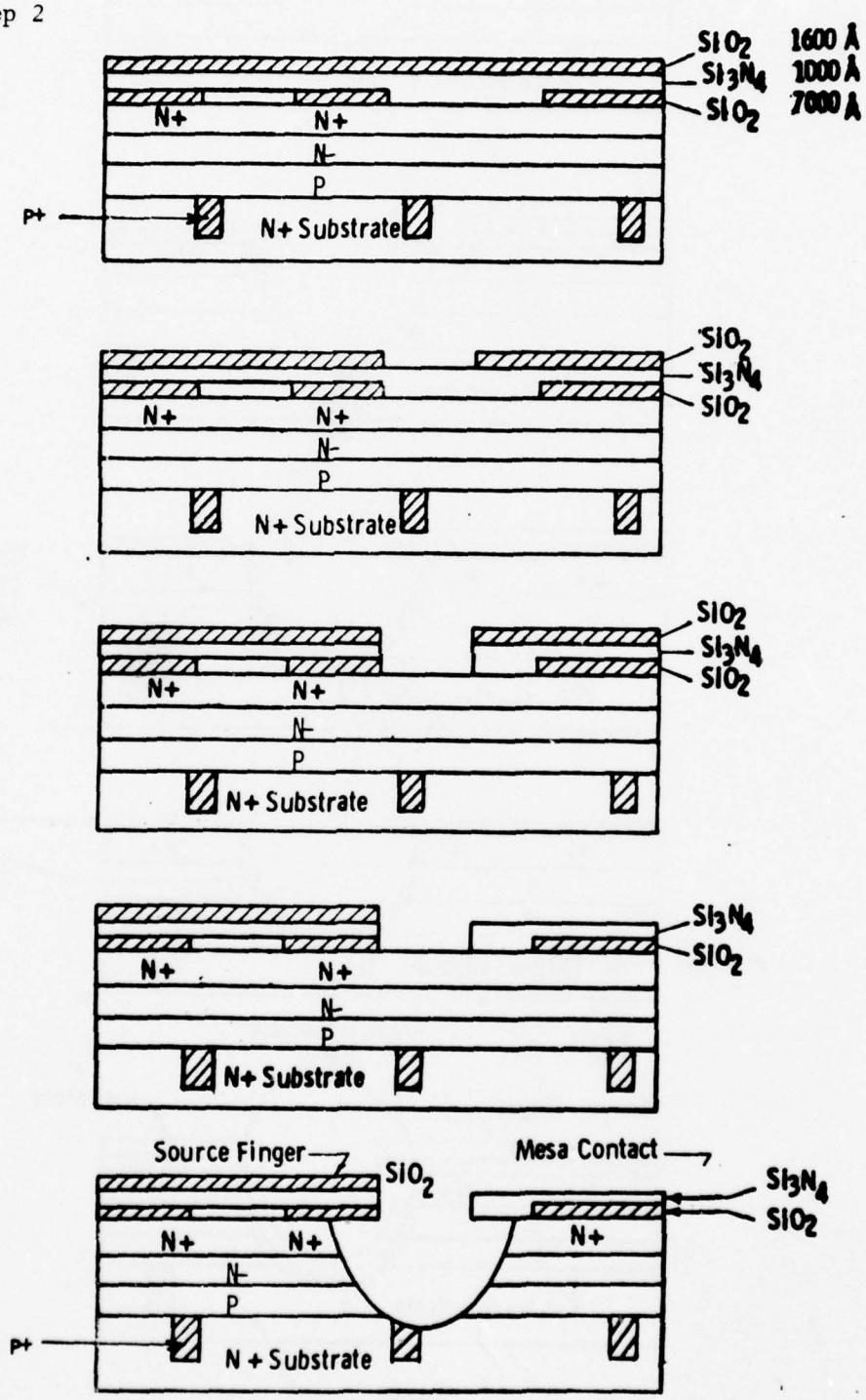


Figure 3.5 Mark VI VMOST Device Fabrication Steps

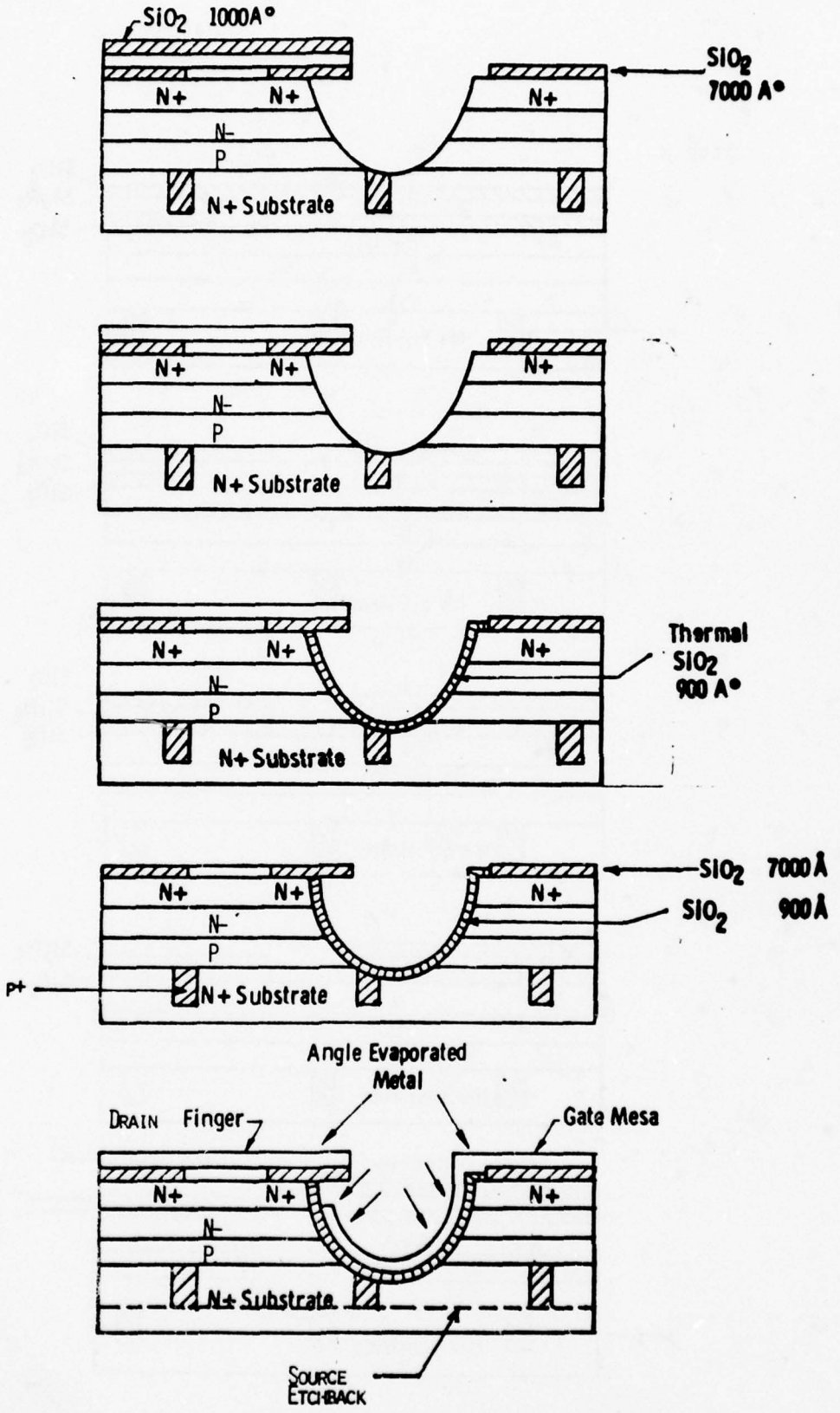


Figure 3.5 (continued)

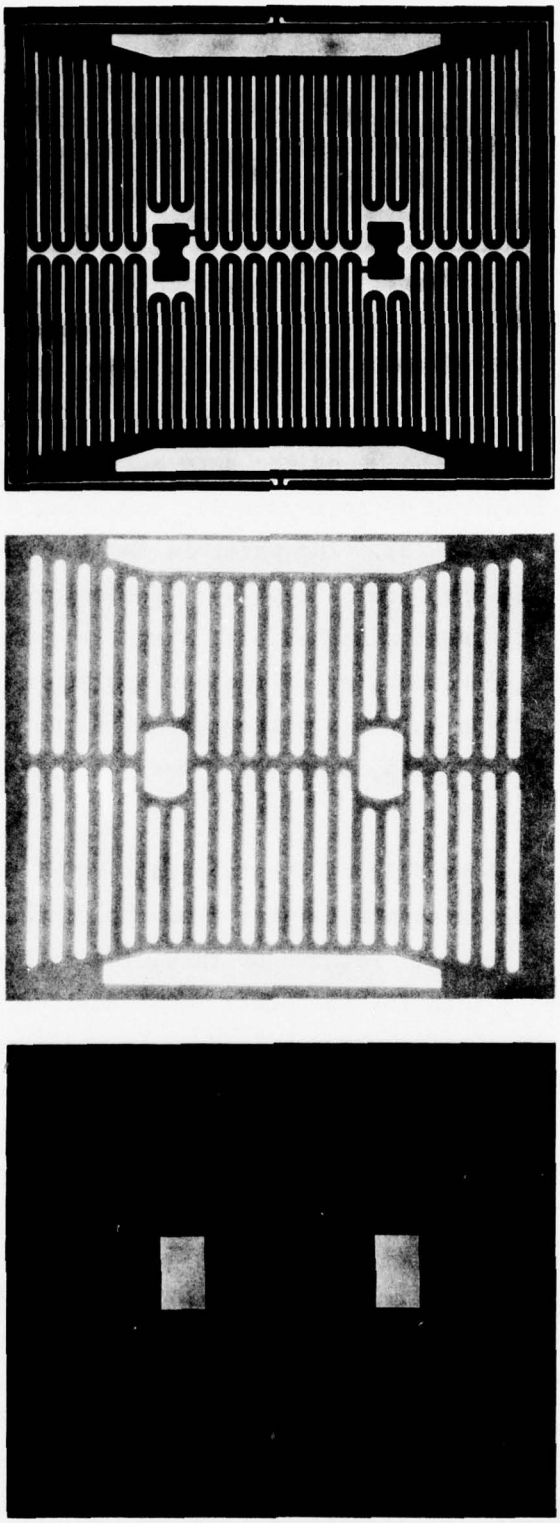


Figure 3.6 Inverted VMOST Masks

Step (3). The wafer is now etched in a commercial phosphoric acid solution (Transetch - N) to remove the Si_3N_4 down to the silicon level, Step (4).

Mask C is used to selectively etch away the SiO_2 layer covering the Si_3N_4, Step (5), on the gate mesa pads. The exposed silicon is then etched to a depth of approximately 5 μm, Step (6), down to the n^+ substrate.

In Step (7), the Si_3N_4 on the gate mesas are removed, followed by a quick etch in buffered HF to remove the remaining SiO_2 mask layer on the drain fingers, Step (8). The wafer is now thermally oxidized to form the thin MOS gate insulator, Step (9). Following this, the Si_3N_4 covering the drain openings is etched off, Step (10), and the gate and drain metal contacts are deposited at the appropriate angle, Step (11). Finally, the front of the wafer is protected while the back of the wafer is etched down to the p^+ slots, Step (11), and metallized to form the source contact.

The epitaxial profile of the top-drain VMOST device is such that the channel p-region is now further from the surface by the thickness of the n^- drift region. Because of this, the gate evaporation angle is lower ($< 60°$) than for the other VMOST devices. More important, a single aluminum evaporation can now be used in place of the multi-metal evaporation scheme without sacrificing the sheet metal resistance, Figure 2.7.

3.2 Mark VII Top-Source V-Groove VMOST Processing

3.2.1 Material Processing. The starting substrate material for the Mark VII Top-Source V-Groove VMOST device was <100> orientation, As-doped, 0.008 Ω-cm silicon. Epitaxial layers of n^- ($\sim$ 3 μm and 10^{15} cm^{-3} concentration), p ($\sim$ 1 μm and 3-5 x 10^{16} cm^{-3} concentration), and p^+ ($\sim$ 1.5 μm and $> 10^{16}$ cm^{-3} concentration) materials were then grown sequentially on the substrate, followed by an n^+ phosphorous diffusion to form the complete transistor profile. As in previous VMOST top-source designs, the depth of the n^+ source diffusion is controlled

to be slightly deeper than the p^+ epitaxial layer to ensure complete channel inversion at the source end.

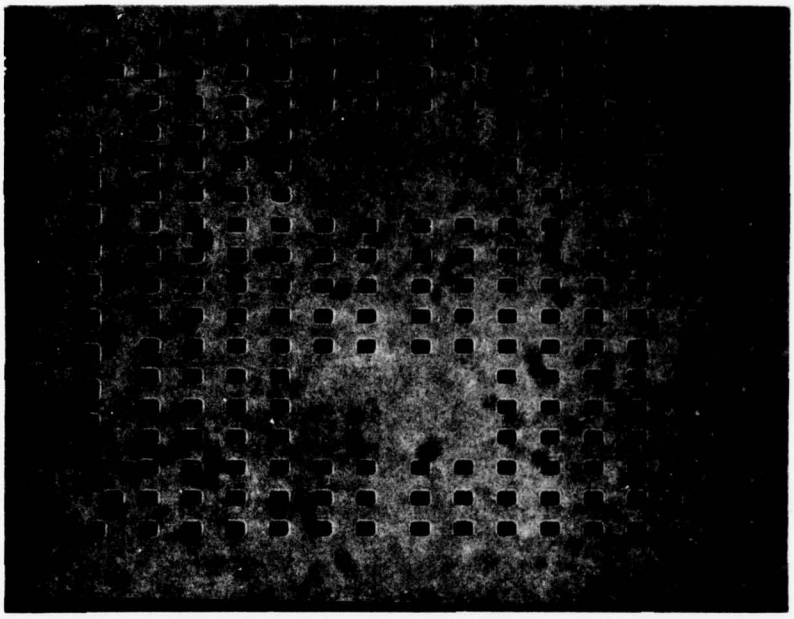
3.2.2 Device Processing. The device fabrication steps of this transistor are very similar to previous VMOST devices (see Annual Report, 1975). Mask A, Figure 3.7, is used to leave p^+ grounding islands in the mesa fingers of the transistor during the n^+ source diffusion. The transistor is defined by Mask B, and Mask C is the Si_3N_4 protection mask which covers the source region during thermal oxidization of the gate insulator. Mask D is used to define the gate mesas for bonding. The slit opening between fingers in Mask B is approximately 1.5 μm to minimize gate-source overlap.

Prior to the formation of the V-grooves, an isotropic silicon etch is used to undercut the oxide and form the overhangs to a length which is predetermined by the slit opening dimension and the location of the p-channel layer in the epitaxial profile. Following this, an anisotropic KOH etch solution is used to create the V-troughs. If the epitaxial profile is correctly matched to the mask dimensions, and the isotropic and anisotropic etch depths are in the proper proportion, then a simple vertical (0° angle) metal evaporation is all that is necessary to form the gate and source contacts.

In the course of the study, a number of different KOH etch compositions were tried in an attempt to minimize etch striations and surface state densities. The latter was found to be critically dependent on the etch composition and the cleaning procedures following etching.

Figure 3.8 shows the top view of a fabricated device just prior to aluminum evaporation. As mentioned earlier, the gate width of this device is approximately 0.9 cm and the active device area is 0.3 mm by 0.39 mm.

(a)



(b)

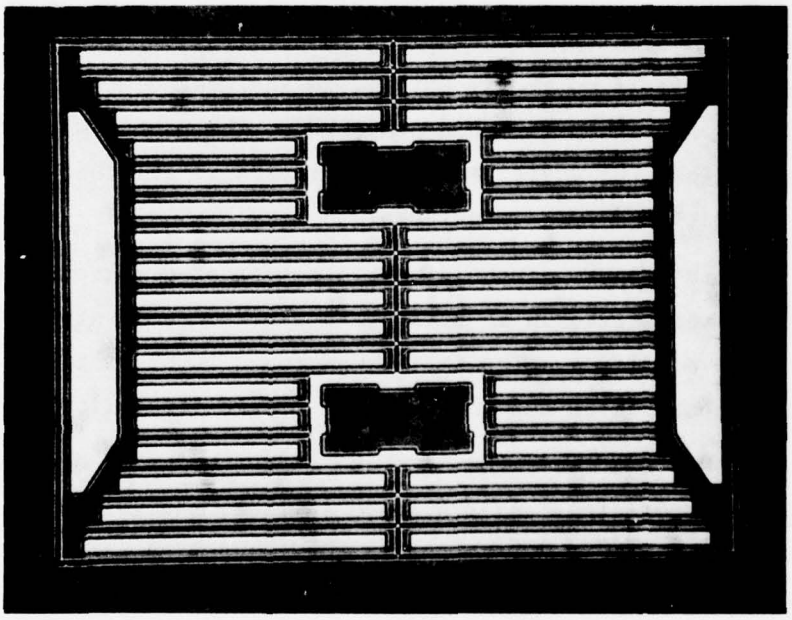
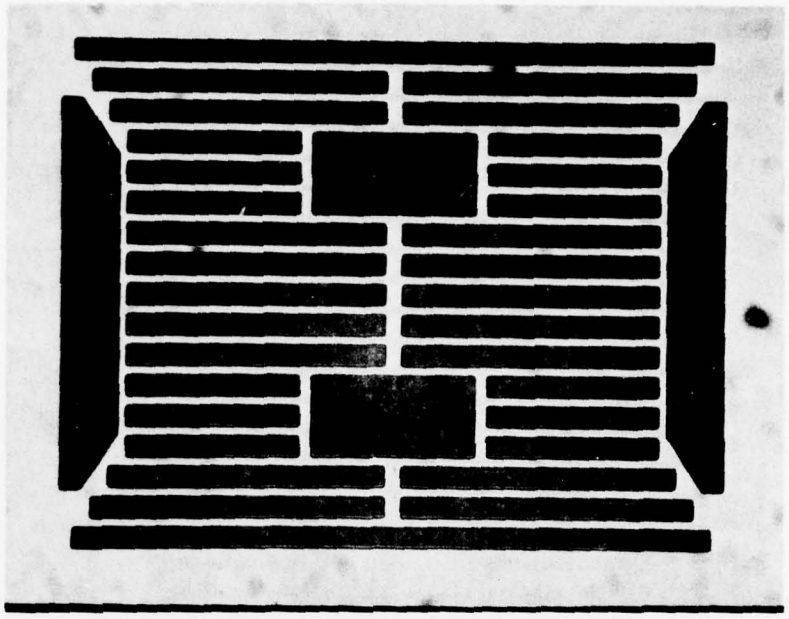


Figure 3.7 Top-Source V-Groove VMOST Fabrication Masks

(c)



(d)

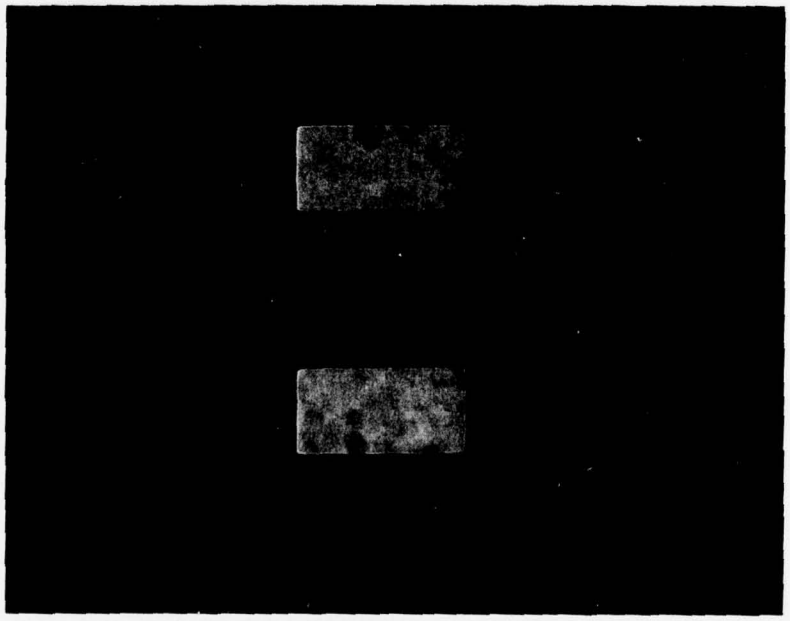


Figure 3.7 (continued)

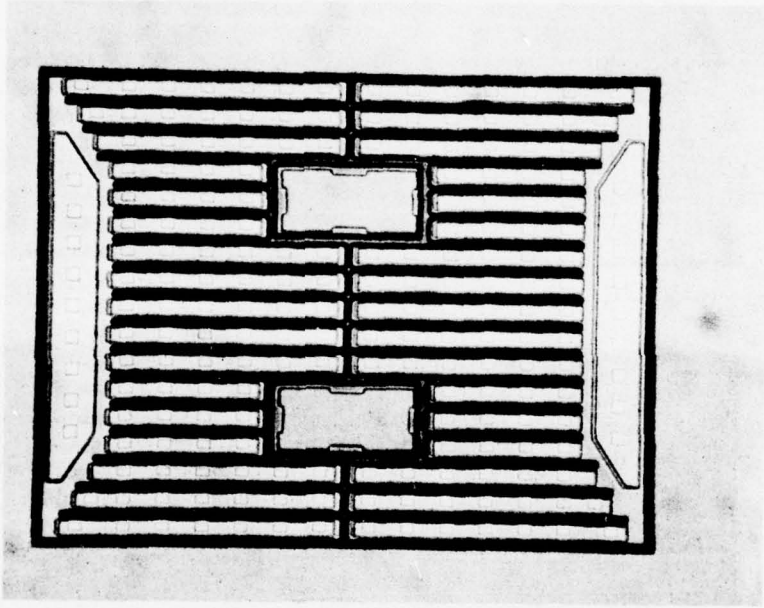


Figure 3.8 Fabricated V-Groove VMOST Device

4. EXPERIMENTAL RESULTS

4.1 Low Frequency Evaluation

4.1.1 Mark VI Top-Drain VMOST. Although the experiments on groove backfilling and polishing were successfully carried out, as discussed earlier in Section 3.1, some difficulties were encountered in growing and evaluating the n^+-p-n^- impurity profile of the epitaxial layers. In the absence of the back-filled p^+ grooves, the growth conditions were fairly normal, and spreading resistance measurements revealed well-defined p and n^- regions suitable for VMOST fabrication, as shown in Figure 4.1.

The presence of the p^+ grooves, however, appear to complicate the epitaxial growth. Figure 4.2 shows the concentration profile of an epitaxial run made on a back-filled <110> As-doped substrate, using similar growths as in Figure 4.1. As expected, there was noticeable out-diffusion of B from the highly doped p^+ grooves, resulting in conversion of the n^- layer to p^- doping. More significantly, the presence of the grooves have a profound effect on the spreading resistance profile, as evidenced by the periodic high resistance perturbations in Figure 4.2. These perturbations are a result of the presence of the grooves, as illustrated in Figure 4.3. At point C, for example, the resistance measured is that of the p^+ groove rather than the n^+ substrate, hence the periodic perturbations. Even at points B and A the groove effect is still quite noticeable. Because of this, an interpretation of Figure 4.2 is extremely complex, and of only marginal value quantitatively.

Experiments to measure the epitaxial profile of a grooved substrate by the capacitance-voltage technique, together with sequential etching were planned, but were unfortunately not carried out because of

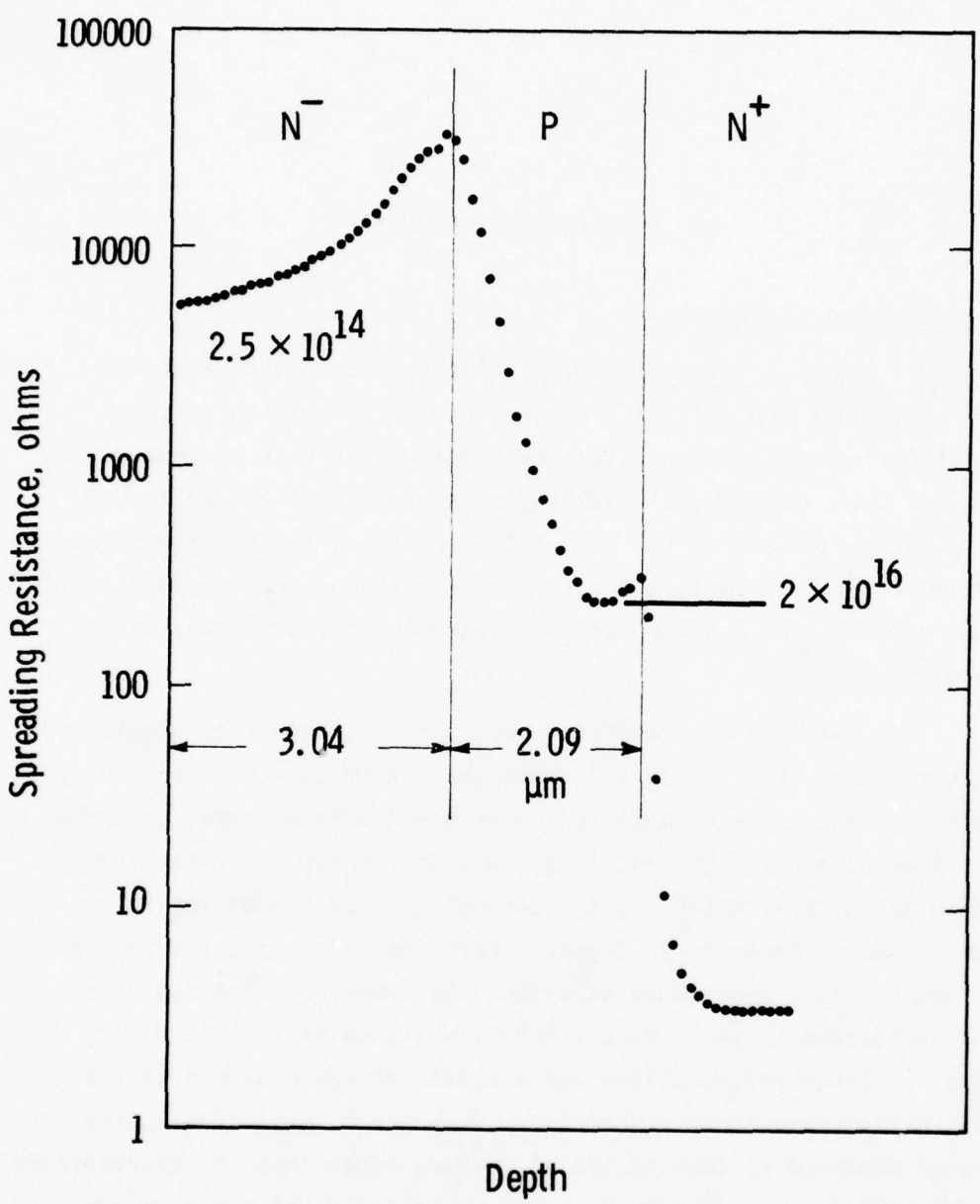


Fig. 4.1 – Epitaxial profile of Mark VI VMOST without groove backfilling

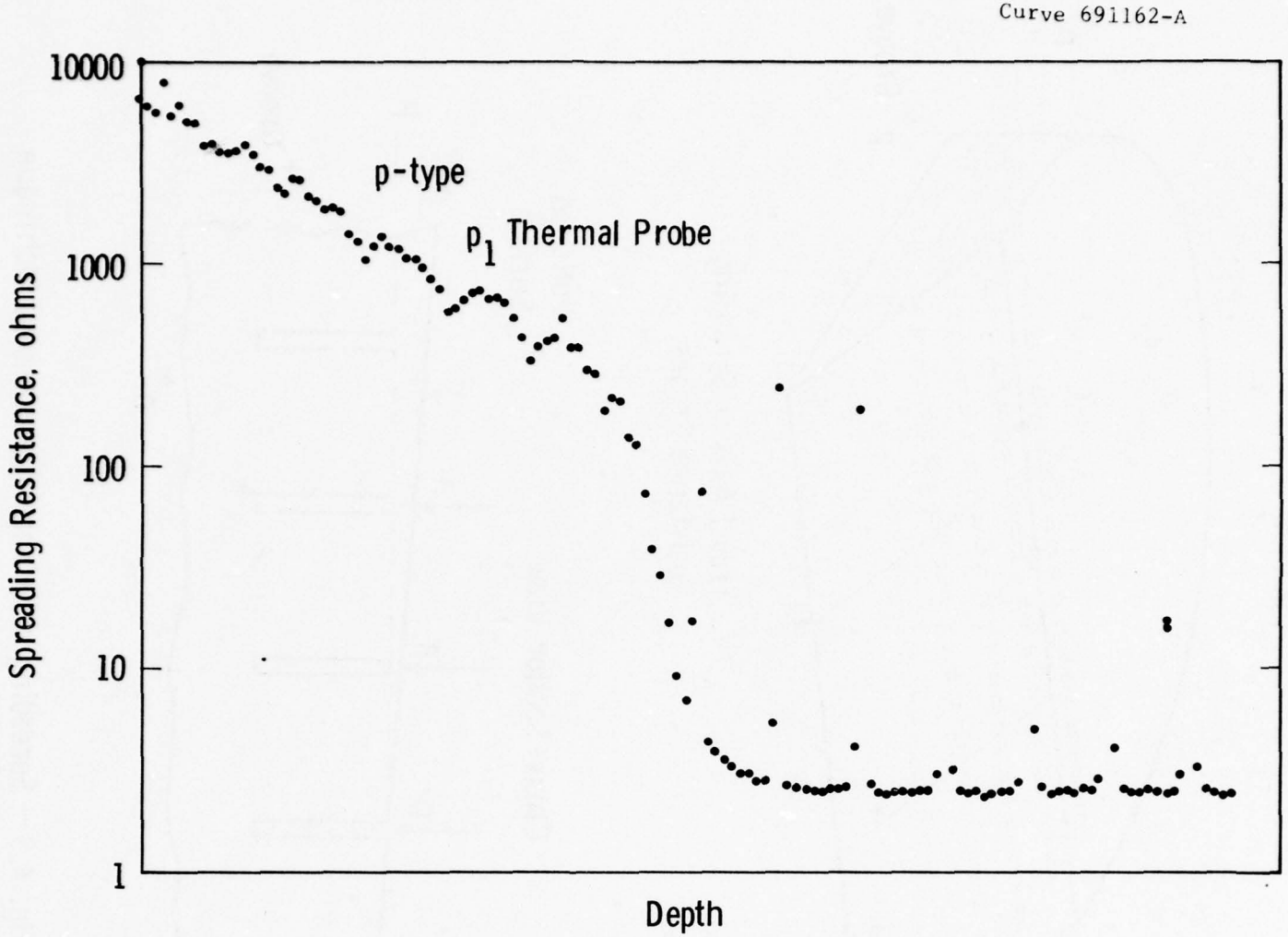


Fig. 4.2 – Epitaxial profile of Mark VI VMOST with backfilled grooves

Dwg. 6415A23

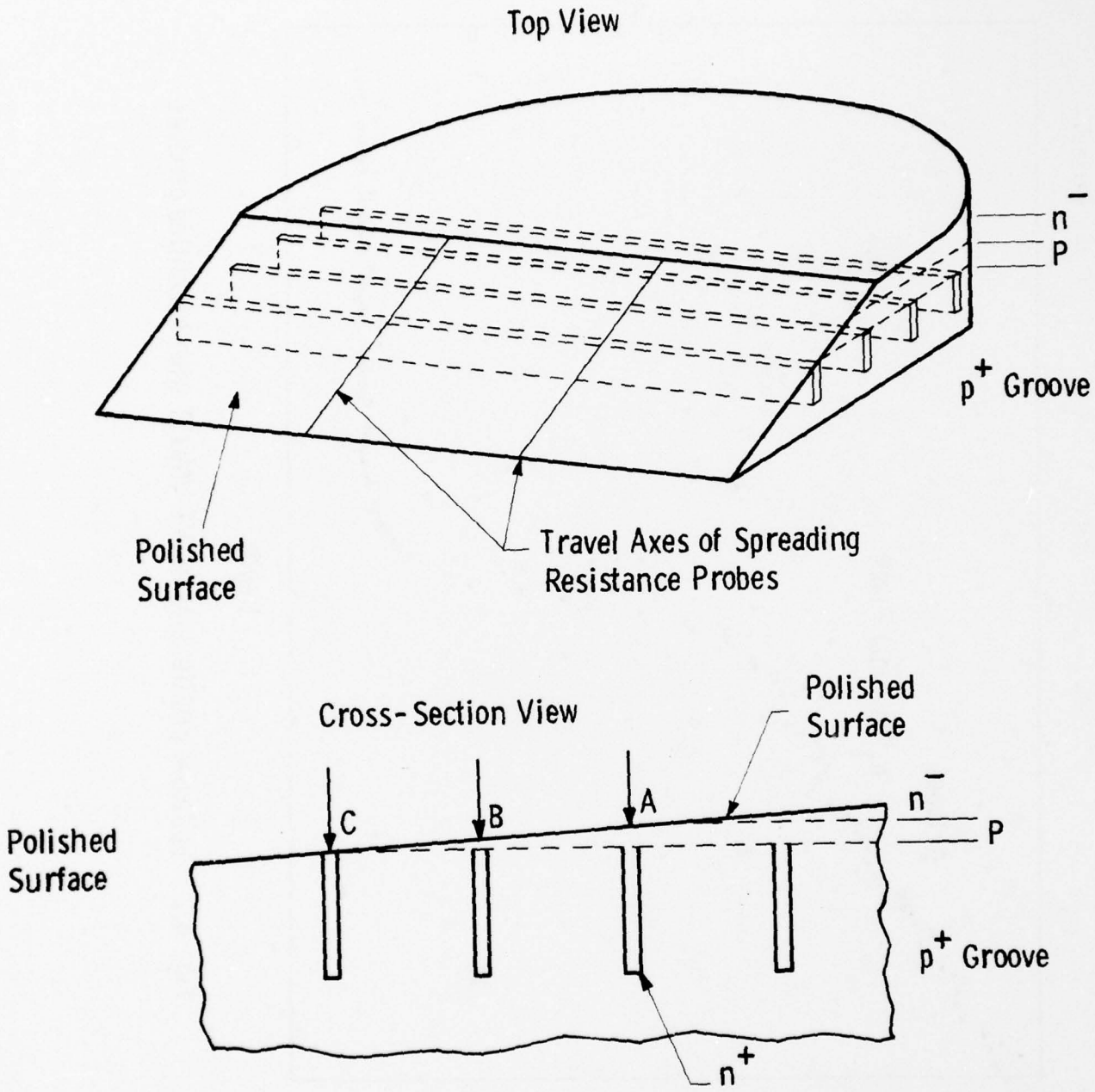


Fig. 4.3 – Spreading resistance measurement technique of Mark VI VMOST

a lack of time. The development of the Mark VI VMOST device was therefore terminated at this point.

The fabrication masks of the Mark VI VMOST were used, however, for the processing of a number of top-source VMOST devices to study the low angle ($< 60°$) evaporation and the feasibility of single metal (Al) source/gate contacts. To achieve the low gate angle, the thickness of the n^+ source epitaxial layer was increased to approximately 3 μm. The results of this series of experiments are described in the next section.

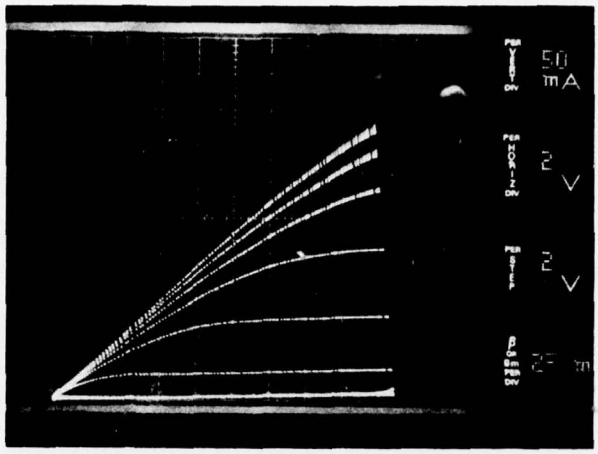
4.1.2 Mark VIII Top-Source V-Groove and Low-Angle Evaporation VMOST Devices. Top-source V-Groove and conventional VMOST devices similar to those reported in the previous final report were successfully fabricated and tested. Since the V-groove device did not have a trough metal bus lying over the drain region, the n^+ predep used in previous VMOST geometries (e.g., Mark V VMOST) was eliminated and a much higher resistivity ($< 10^{15}cm^{-3}$) n layer was grown to minimize C_{GD} and C_{DS}. This also ensured a rapid depletion of the n^- region with drain voltage during operation to enhance the RF gain of the device and minimize the output nonlinearities. The result of the high n^- resistance can be seen in the current-voltage characteristic of one such device in in Figure 4.4a. The turn-on resistance of this device was over 40Ω which greatly reduced the available rf voltage swing of the device when used as a power amplifier. As will be discussed in Section 5, this turn-on resistance is attributed to the space-charge resistance of the n^- region, and by increasing the concentration of this layer (Figure 4.5) a substantial improvement of the drain characteristics was achieved, as shown in Figures 4.4b and 4.4c.

The 0.9 cm gate periphery V-groove devices showed breakdown voltages in excess of 25V, gate breakdown voltages of over 50V and dc transconductances of approximately 80 mmho. These values are in good agreement with the expected performance of the device.

Conventional low gate angle 1.76 cm gate width top-source VMOST devices with high n^- resistivity also exhibited the same large

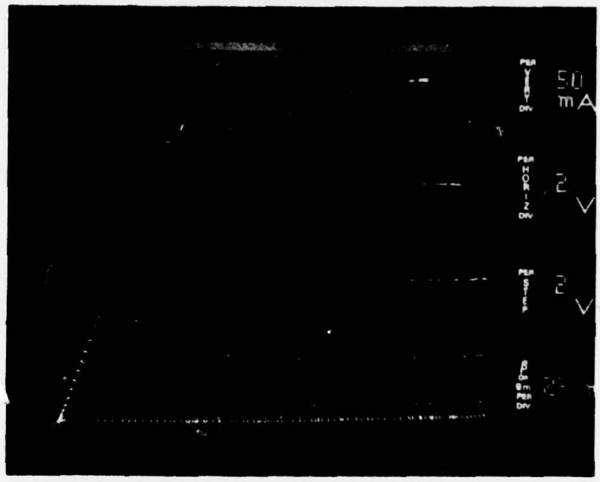
(a)

low n^- conc.
high R_{on}
#37-2



(b)

higher n^- conc.
lower R_{on}
#41-2



(c)

Same as (b)
#41-2
(5V/div)

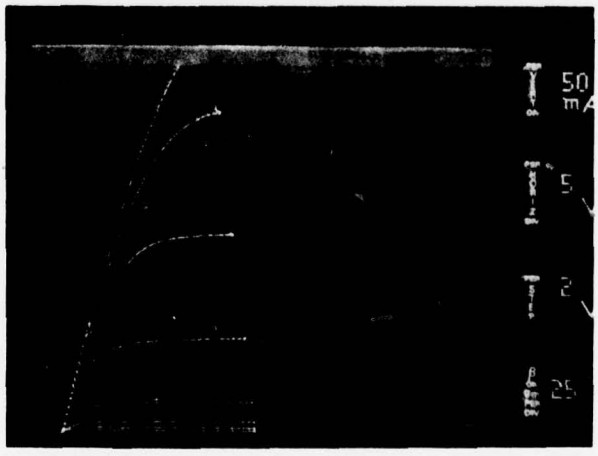


Figure 4.4 I-V Characteristics of V-Groove VMOST

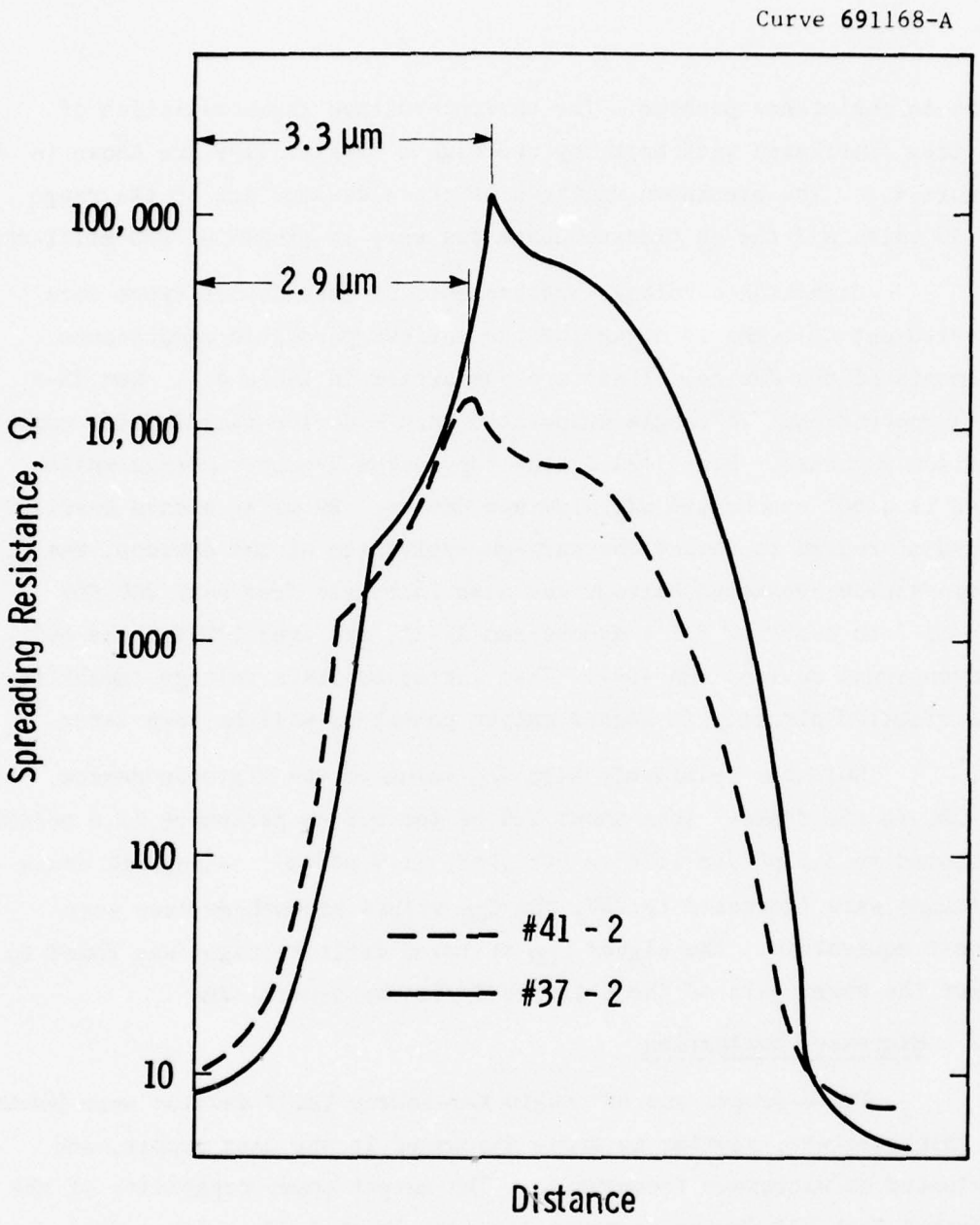


Fig. 4.5 – Spreading resistance profiles of VMOST runs #37 - 2 and #41 - 2.

turn-on resistance problem. The current-voltage characteristics of devices fabricated with both low and high n^- resistivity are shown in Figure 4.6. The breakdown voltages of these devices are in the range of 50 volts and the dc transconductances were in excess of 200 milli-mhos.

Capacitance-voltage measurements of both device types were carried out at 1 MHz to determine the various parasitic capacitance elements of the device. These are summarized in Table 4.1. Run 33-3 is a conventional 78° angle evaporated Mark V device included for comparison purposes. Run 41-2A is the top-source V-groove design while 42-3 is a 60° evaporated all aluminum device. By using a more heavily doped n^- region to reduce the turn-on resistance of the devices, the drain-source breakdown voltage was also increased from near 20V for run 33-3 to over 30V for V-groove run 41-2A, and over 50V for the 60° conventional device, run 42-3. This increased drain voltage capability has resulted directly in higher output powers as will be seen later.

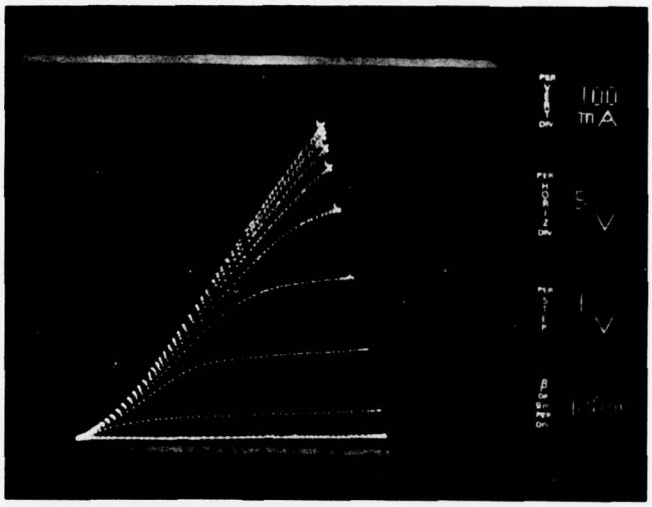
Note the relatively high C_{GD} value of the V-groove device, 41-2A, in the table. This shows 2.5 pF for 0.9 cm periphery (2.8 pF/cm) compared to 3.3 pF for 1.76 cm periphery (1.9 pF/cm). When both drain voltages were increased to 25V, the C_{GD} values of both devices were almost equivalent. The higher C_{GD} at lower drain voltages was found to lower the power gain of the V-groove device by several dB.

4.2 Microwave Evaluation

The V-groove and 60° angle top-source VMOST devices were bonded on chip carriers, similar to those discussed in the last report, and evaluated at microwave frequencies. The output power capability of the V-groove Mark VII device is typically over 1W at 1 GHz with a drain efficiency of 17% (Class A operation). The small signal gain was in excess of 6 dB at this frequency.

In small signal S-parameter testing, the gain of the V-groove device was heavily dependent on the drain voltage. At V_{DS} = 15V, the device had only 2 dB gain, while at 25V it increased to 7 dB. This gain dependence on V_{DS} is due to the slowly decreasing dependence of C_{GD} with drain voltage in

(a) high
n^- resistance



(b) lower
n^- resistance

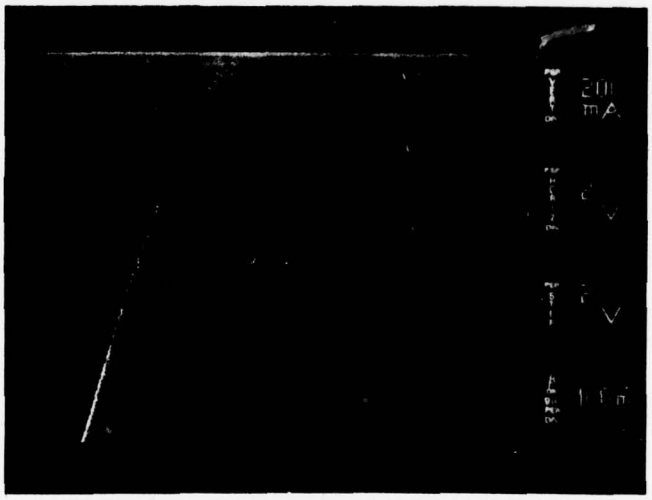


Figure 4.6 I-V Characteristics of 60° Angle Evaporated VMOST

Run # Type Periphery	Metal Scheme	Physical Dimensions			Capacitances							G_m
		L Channel	N^- Conc.	N- Width	C_{GD} 10V	C_{GD} 25V	C_{GS} 10V	C_{GS} 25V	C_{DS} 10V	C_{DS} 25V	C_{DS} 50V	
#33-3 VMOST Mark V 1.7 cm	78° Cr Pd Au	.85μ	2.5×10^{15} cm^{-3}	1.5μ	6.5 pF		16.5 pF		15.5 pF			250 mmho
#41-2A V-G-MOST Mark VII 0.9 cm	0° Al	1.26μ	3×10^{15} cm^{-3}	1.2μ	2.5 pF	1.78 pF	12.2 pF	12.9 pF	5.4 pF	3.5 pF		80 mmho
#42-3 VMOST 1.7 cm	60° Al	1.0μ	4×10^{15} cm^{-3}	3μ	3.3 pF	2.7 pF	17.0 pF	17.6 pF	16.7 pF	12.3 pF	8.1 pF	230 mmho

TABLE 4.1 Typical Measured Characteristics of Three VMOST Types

these devices, as shown in Figure 4.7. Since the intrinsic maximum stable gain (MSG) of the device can be expressed as

$$MSG = \frac{gm + jw\ C_{GD}}{jw\ C_{GD}}$$

it is easy to see the dependence of gain with C_{GD}.

The power output of a Mark VIII device from run 41-2A is shown in Figure 4.8 at drain voltages of 25V and 30V. Over 1 watt was achieved at 30V with 4 dB gain and 17% drain efficiency. This corresponds to a power-added efficiency of only 10%. At 25V, the output power at the 4 dB gain point was even lower (0.5W) and the drain efficiency was 12%. Nevertheless, these powers are the highest known values for a V-groove type MOST device at 1 GHz.

The low power and efficiency of the V-groove device are clearly caused by the high turn-on resistance ($\sim$ 13Ω) which limits the available power triangle. With proper design, the device is capable of producing up to 3W if the turn-on resistance is down to 4Ω, as expected for this periphery.

Thus, although the gain and power of the V-groove device were lower than expected, it clearly demonstrates the potential of the (W) V-groove technology in which oxide overhangs are used to limit the gate-source overlap and extend the usable frequency range of V-groove devices to above 1 GHz.

By comparison, low angle VMOST devices were found to produce up to 10W of rf power at 1 GHz, and at a useful gain of 6 dB. The power-added and drain efficiencies were typically over 30%, and 50% respectively, and the small signal gains were in excess of 10 dB. These results are shown in Figure 4.9. For comparison the output power capability of a conventional Mark V VMOST device, # 34-3-7, is shown in Figure 4.10. The small signal gain of this device was over 13 dB; the power added and drain efficiencies were 33% and 38% respectively at the 4W output power point.

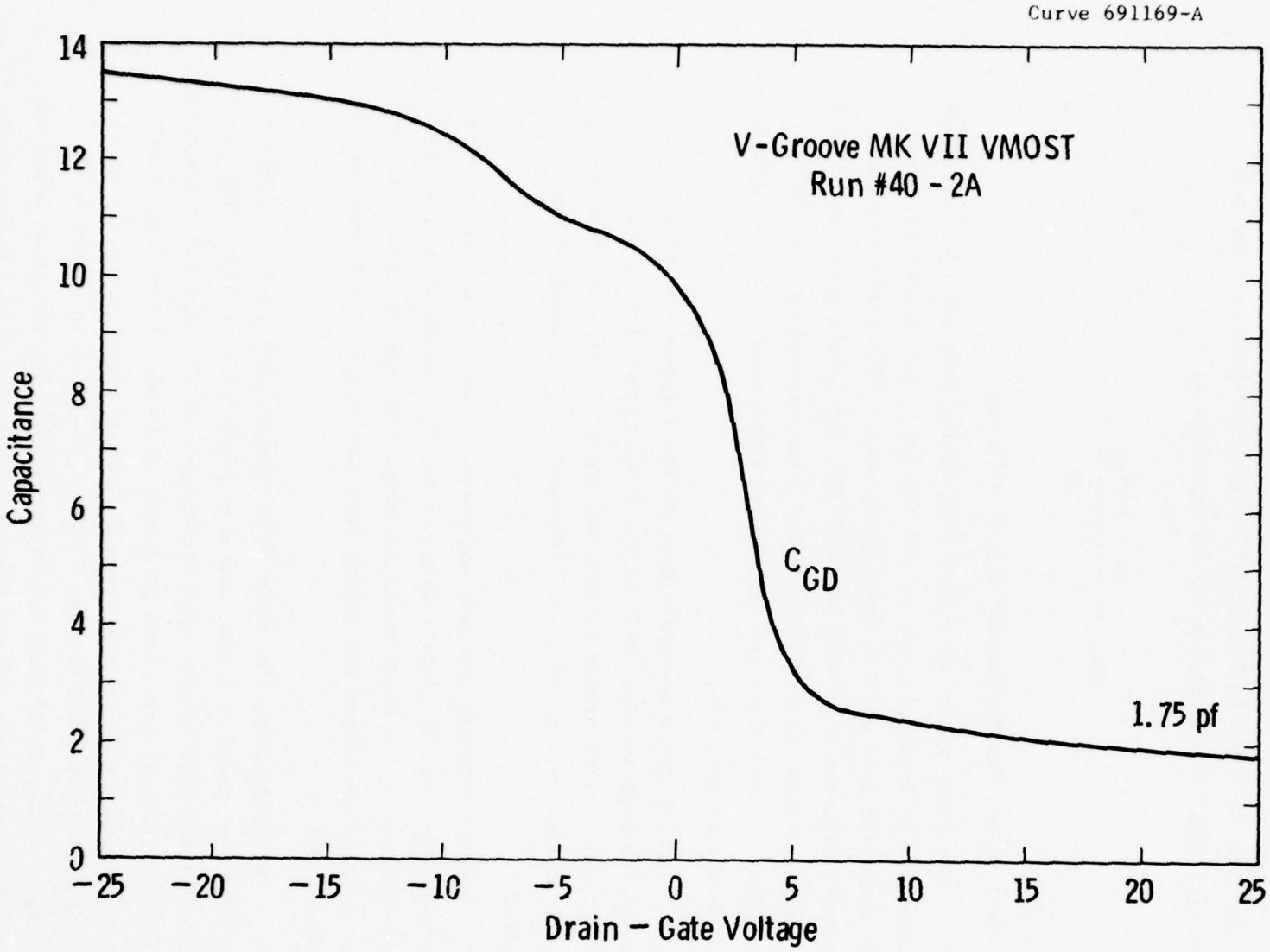


Fig. 4.7 – Variation of C_{GD} with gate-drain voltage, V-groove MK VII VMOST device.

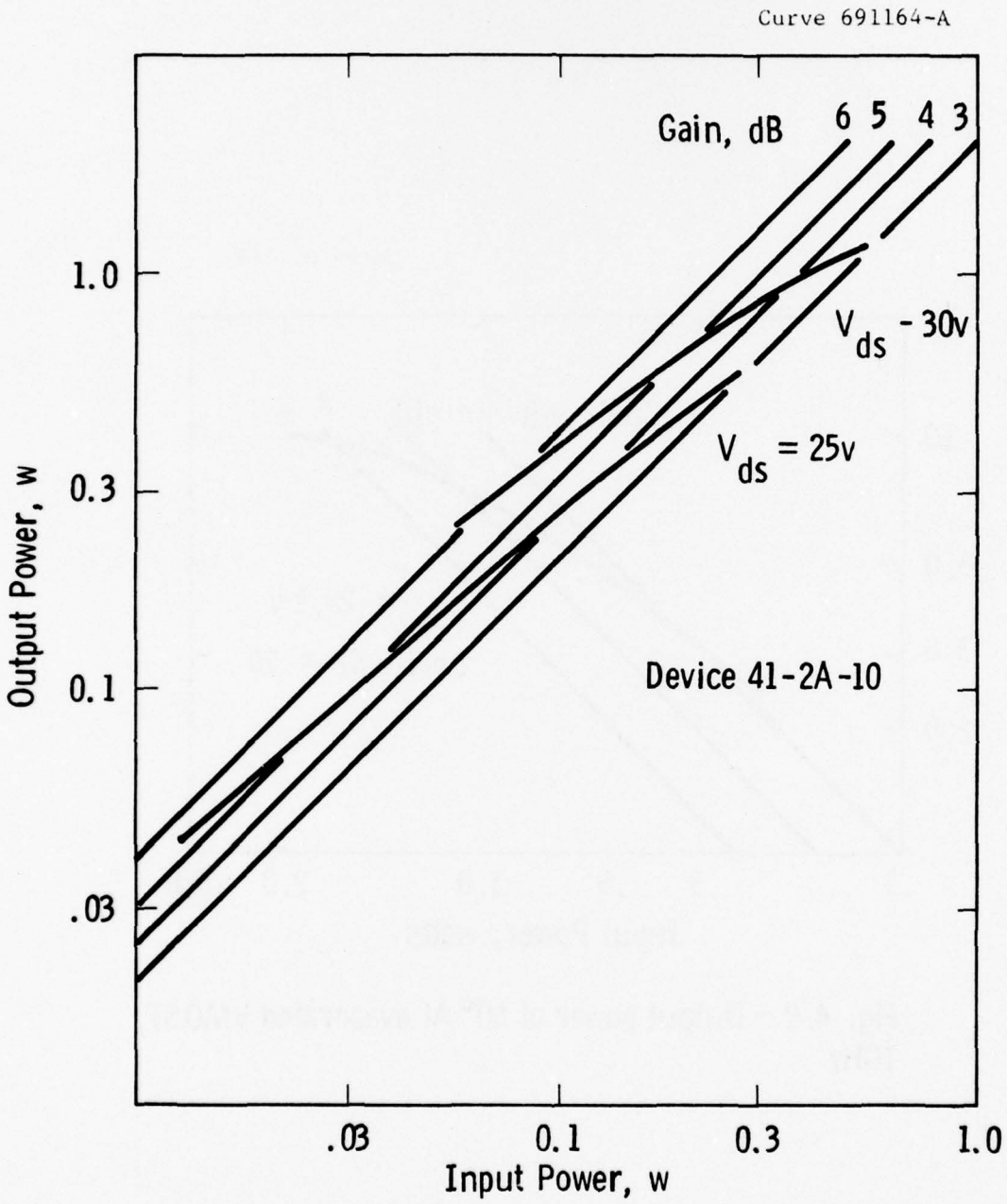


Fig. 4.8 — Output power of V-groove, MK VII, MOS-transistor at 1 GHz

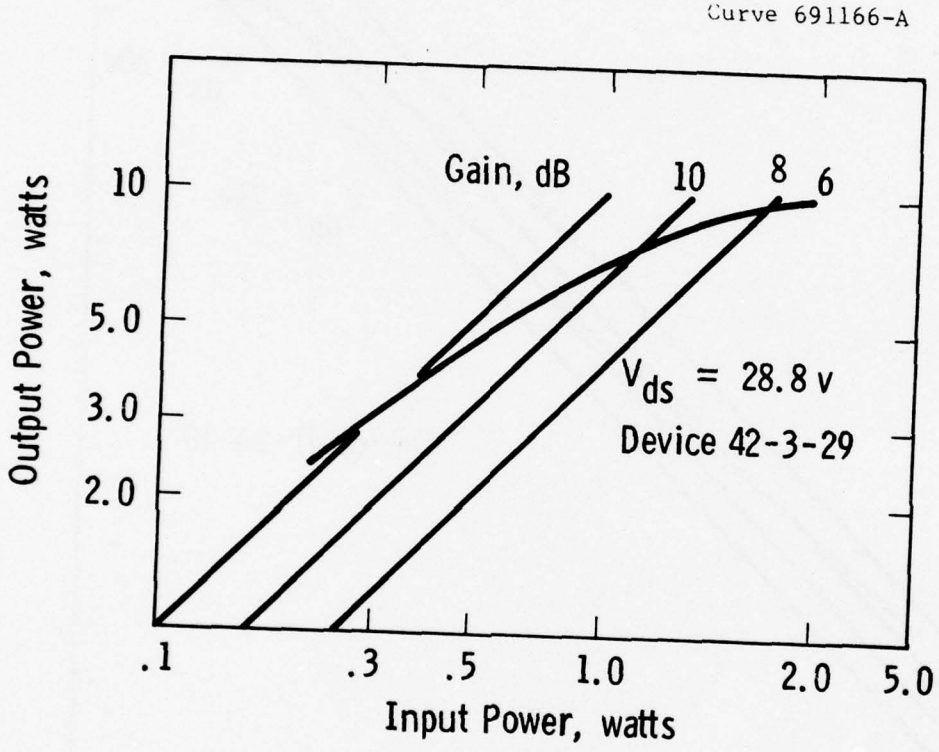


Fig. 4.9 – Output power of 60° Al evaporated VMOST, 1GHz

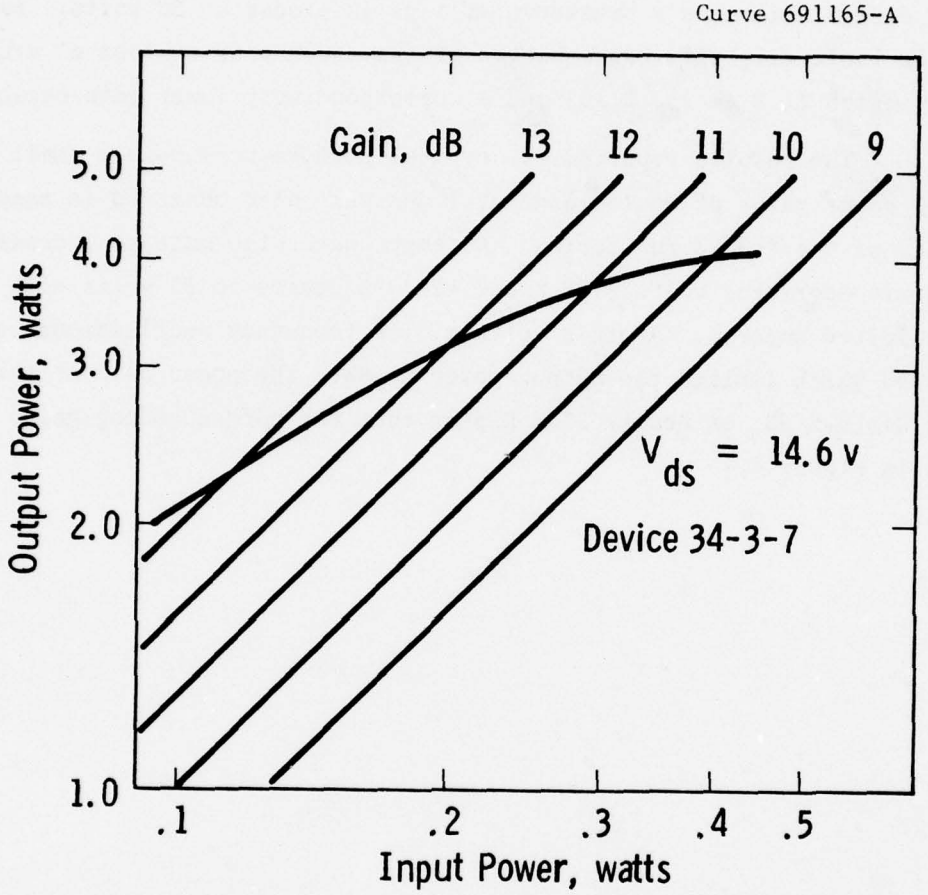


Fig. 4.10 – Output power of conventional 78° VMOST, 1 GHz

The one significant difference between the two devices in Figures 4.9 and 4.10 is the drain voltage capability of the low angle VMOST design which has a breakdown voltage in excess of 50 volts. As seen in Table 4.1, this was achieved at the expense of a wider n^- drain drift region (1.5 μm vs. 3 μm) and a correspondingly lower gain capability.

The results reported are typical performances, since small signal power gains of up to 16 dB at 1 GHz were also observed in some devices of the # 34-3 run series. Attempts were also made to increase the drain operating voltage of the # 42-3-29 device to 35 volts with only limited success. At this voltage, low frequency oscillations were observed which limited the output power to 8W. The power gain at this point was 9.5 dB, or nearly 2 dB higher than the corresponding gain shown in Figure 4.9.

5. DISCUSSION

5.1 Power-Frequency Performance

The work that has been carried out to date under Contract N00014-74-C-0012 has shown that short gate (1-2 μm), large periphery (0.9-1.76 cm gate width) vertical channel enhancement mode MOS transistors (VMOST's) can be fabricated in silicon with reasonably high yields (> 50%) to operate at frequencies up to 4.5 GHz. As such, these devices have useful power gains at frequencies below 2 GHz for linear amplifier applications. The turn-on resistance of the VMOST device (0.6 to 1 ohm per unit cm gate periphery) is also significantly lower than any MOST device available at present, and opens up the possibility of using the transistor for switching applications where the absence of second breakdown is a distinct advantage, e.g., switching of inductive loads.

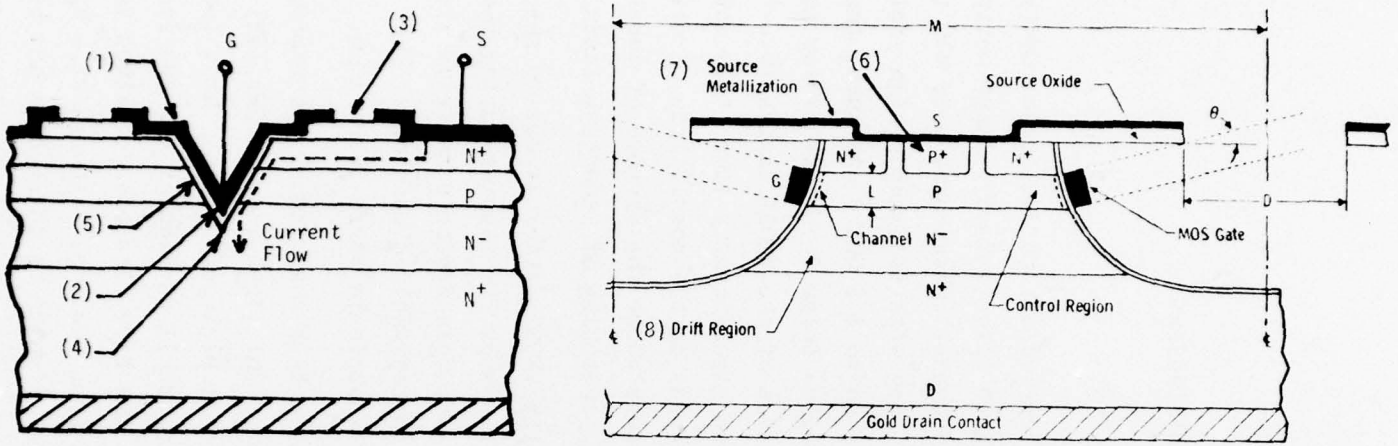
Much of the success of the VMOST device is due to the VMOST technology which utilizes oxide overhangs for masking during the gate evaporation. In this manner the extrinsic device parasitics are kept to a minimum without invoking small photographic dimensions. The minimum device mask dimension for example is never below 3 μm.

The power levels that have been achieved by the various VMOST geometries are state-of-the-art at 1 GHz (10W) and 1.5 GHz (6W) respectively. From a gain-product per unit periphery basis, these translate to values of approximately 35 dB-W/cm and 11 dB-W/cm at the two frequencies. Values as high as 45 dB-W/cm at 1 GHz have also been obtained in the VMOST device discussed in the previous section, although at a slightly lower power (8.2W). By comparison, a value of 14 dB-W/cm has been reported by Morita et al.[1] at 1 GHz for an n-channel planar depletion-type Si MOST with a 2 cm gate periphery.

---

(1) Y. Morita, H. Takahashi and M. Fukuta, IEEE Trans. Electron Devices, Nov. 1974, Vol. ED-21, No. 11, p. 733.

HIGH-FREQUENCY VERTICAL CHANNEL MOSTS



V-GROOVE MOST

(W) VMOST

PROBLEM AREA	DEVICE INFLUENCE
(1) Gate-Source Overlap	Excess Input Capacitance
(2) Gate-Drain Overlap	Excess Feedback Capacitance
(3) Metal Etching Delineation	Spreading resistance in Source, Excess Output Capacitance
(4) Groove Depth	Drain Saturation Voltage, Breakdown Voltage
(5) Surface Morphology	Channel Mobility, Surface States
(6) P^+ Grounding	Output Conductance
(7) Angle Evaporated Metal	Excess Source Contact Resistance
(8) Drain Drift Region	Drain Saturation Voltage, Breakdown Voltage, Output Capacitance

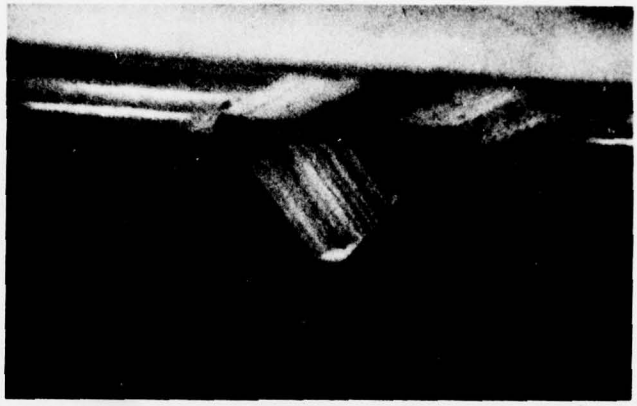
Figure 5.1 Problems of Vertical Channel MOST Devices

5.2 Processing Technology

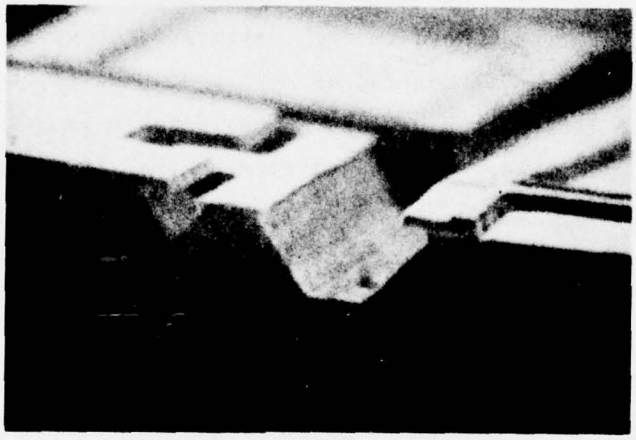
In comparison with other vertical channel technologies, more specifically the V-groove VMOS technology, the Westinghouse VMOST technology at first appears to be more involved. This is only true of the device geometry, not the processing steps, where the need for a metal delineation of the source and gate contacts (such as required in VMOS devices) has been eliminated. The source, gate, and drain contacts are automatically defined in a single vacuum pump-down. Some of the problem areas, however, are similar to both technologies, as illustrated in Figure 5.1.

The gate-source overlap problem in the conventional V-groove MOST has been eliminated to a large extent in the (W) VMOST. The problem of gate-drain overlap in contrast is common to both since in practice this will always exist, and in some cases it may even be necessary (see Section 5.3). There is no need to etch delineate the gate and source metal contacts in the VMOST device, as mentioned earlier, and the surface morphology of the latter is excellent. Considerable improvements in the V-groove surface morphology can be achieved however by using a 100% KOH solution at room temperature, as shown in Figure 5.2. The principal advantage of the anisotropic KOH etch is that it is self-limiting, i.e., the groove depth is uniformly defined by the initial mask opening. On the other hand, some care must be exercised in the VMOST device to ensure the correct etch depth and oxide undercutting for a given epitaxial profile. Unfortunately, the potassium-based anisotropic etch solution is a serious source of oxide contamination and modifications of normal processing procedures may have to be made to overcome this problem.

Table 5.1 summarizes the results obtained from a detailed study of the gate oxide contamination problem carried out during the course of the (W) V-groove, Mark VII, VMOST device development. The standard KOH:IPA etch solution was found to give rise to a striated etch surface, Figure 5.2, and to a high density of oxide charge, $N_{OX} > 10^{12}$ cm^{-2}. Prior to gate oxidation the surface was rinsed thoroughly in DI, and oxidized to a thickness of 200Å. This oxide was then stripped and a new



KOH + ALCOHOL ETCH



SMOOTH WALL ANISOTROPIC ETCH OF 100% KOH

Figure 5.2 V-Groove Surface Morphology Dependence on KOH Composition

TABLE 5.1

(W) V-GROOVE MOST PROCESSING DATA

Etch	Surface Morphology	Oxide (1,000 Å)	Temp. (°C)	Anneal (400°C, 60 min)	V_{FB} (VOHS)	N^*_{ox}, cm^{-2}
Standard KOH:IPA + DI Rinse + Pre-Oxidation	Striated	HCℓ (Dry) HCℓ (Wet) O_2 (Wet)	1,000 1,000 950	H_2 H_2 H_2	> -25 > -25 -3.8	Bad ($>10^{12}$)
(W) KoH Soln. + DI + Pre-oxidation + C3B Preclean	Smooth	HCℓ (Dry) HCℓ (Wet) O_2 (Wet)	1,000 1,000 950	H_2 H_2 H_2	-2.5 -6.4 -2.1	$< 10^{10}$ 3×10^{11} 8×10^{10}
No C3B Preclean	Smooth	O_2 (Wet)	950	H_2	-3.9	$\sim 10^{12}$

* Thermal Stress - 250°C, 5 min, + 10V.

oxide grown to form the MOS gate insulator at a temperature between 950 to 1000°C. Following the gate metal deposition, the sample was annealed at 400°C for 60 min in an H_2 ambient. In all cases the results were uniformly bad.

By going to a 100% KOH etch solution, followed by DI rinse, pre-oxidation and strip, and finally a proprietary Westinghouse C3B preclean procedure, N_{OX} values as low as 10^{10} cm^{-2} were obtained after the H_2 anneal. The results also indicate that the C3B Preclean is almost mandatory to achieve low N_{OX} values.

(The N_{OX} values were determined by measuring the flatband voltage shift of the MOS-gate capacitor after it has been subjected to a thermal stress of + 10V at 250°C for 5 minutes.)

5.3 Model for Drain Resistance

The low voltage turn-on resistance of vertical channel MOST devices appears to be dependent on a number of parameters: (i) the gate-drain metal overlap, (ii) the resistivity of the n^- drift region, and (iii) the length of the drift region. In devices where punch-through of the n^- region occurs at a very low drain voltage, and where the gate electrode overlap of the drain region is minimum, as in shallow V-groove VMOST devices, the turn-on resistance is anomalously high. This was shown earlier in Figure 4.4a. The high source-drain resistance cannot be accounted for simply from a low voltage consideration of the channel conductance and the remaining undepleted resistance of the n^- region. Furthermore, the anomalous resistance is attributed to the drain, since in Figures 4.4a and 4.4b the dc transconductances were barely affected in both devices.

To account for this, a model is suggested for high power vertical channel MOST devices in which the low voltage turn-on resistance is due to space-charge effects in the n^- region, giving rise to a space-charge resistance component, R_{SC}, which is series with the channel. The value of R_{SC} may be approximated by the expression

$$R_{SC} \sim \left\{ \frac{(L_n - \delta)^2}{2\zeta(W)\varepsilon_s v_{sat}} \right\} \tag{5.1}$$

where W is the active length of each groove, v_{sat} is the saturated carrier drift velocity, and L_n, δ, and ζ are as defined in Figure 5.3.

The width ζ is defined by the effective width of the two intersecting channels at the apex of the V-groove, as shown in Figure 5.3. An exact calculation of this width requires a numerical computer solution of the field distribution in the apex region, which is beyond the scope of the present work. In its place we have used the data from a number of V-groove Mark VII runs in which the depth of the V-groove had been varied to obtain the experimental turn-on resistances at $(V_G - V_T) = 20V$ given in Figure 5.3. The concentrations of the n^- region in all the runs were nominally below 10^{15} cm^{-3}, and the effective n^- thickness was approximately 2 μm. The concentration and length of the p-region were maintained invariant in each case, at least within experimental means.

If we assume in the model that the total source-drain resistance before current saturation is given by the expression

$$R_T = R_C\left(\frac{1}{2N}\right) + R_{OL}\left(\frac{1}{2N}\right) + R_{SC}\left(\frac{1}{N}\right) \tag{5.2}$$

where R_C is the active gate channel resistance; R_{OL} is the extended channel resistance due to the gate overlap of the n^- region; R_{SC} is the space charge resistance given by Eq. (5.1); and N is the number of V-grooves in the device; then

$$R_T = C + A\delta + B(L_n - \delta)^2 \tag{5.3}$$

since R_C is independent of δ, and

$$R_{OL}\left(\frac{1}{2N}\right) \simeq \left(\frac{1}{2N}\right)\left(\frac{\delta}{\sin 54.7^\circ}\right)\left(\frac{1}{W\ {}_N C_i (V_G)}\right) . \tag{5.4}$$

Thus, from Eq. (5.4), (5.3), and (5.1),

$$A = \left(\frac{1}{2N}\right)\left(\frac{1}{\sin 54.7}\right)\left(\frac{1}{W\mu_n C_i V_G}\right)$$

$$B = \left(\frac{1}{N}\right)\left(\frac{1}{2\zeta W\epsilon_s V}\right) . \qquad (5.5)$$

Using Eq. (5.3) and the experimental data points of Figure 5.3, an approximate fit was obtained which showed reasonably good agreement, especially at large δ values. The discrepancy at very low δ values, e.g., δ = 0.1 μm, is probably due to discrepancies in depth measurements. It is also possible that the higher turn-on resistance of the δ = 0.1 μm point may in fact be actually due to an insufficient etch depth, i.e., the groove has not penetrated completely past the p-region. This results in an additional resistance because of a non-inverted or lightly inverted p-layer adjacent to the channel under the V-groove apex. The numerical values of the A, B, and C constants are: A = 6 ohm/μm, B = 12 ohm/μm^2, and C = 2 ohm. These coefficients imply an effective active channel mobility of 360 cm^2/v-s and an effective width ζ of approximately 0.9 μm, both of which are fairly reasonable from very simple considerations of device physics.

In formulating this simple model to explain the turn-on resistance problem in VMOST-type devices, a number of approximations were made. These are explained in Figure 5.4. The longitudinal (x) field distribution at low drain voltages ($2 < V_D < V_{Dsat}$) for very low n^- concentration is assumed to be as shown in Figure 5.4b. Essentially all the voltage drop is seen to take place in the region (L_n-δ) and $E(x) > E_{crit}$ (the critical field required for electron drift velocity saturation, $\sim 10^4$ v/cm). This punch-through situation will take place for V_D = 2v if n^- is less than 6 x 10^{14} cm^{-3} and L_n = 2 μm. Under this condition the space charge effect analyzed earlier is fairly well pronounced.

Curve 691167-A

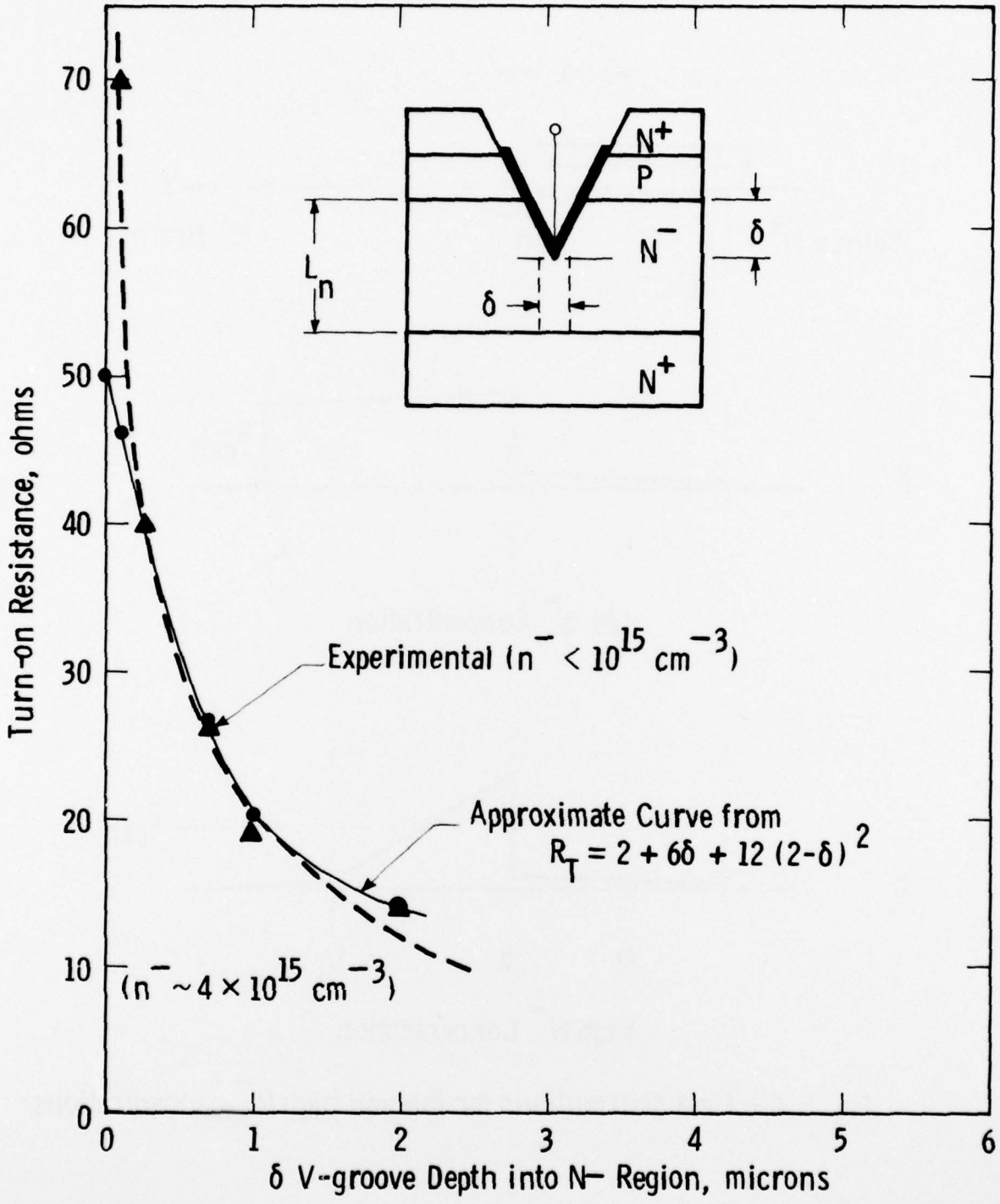


Fig. 5.3 – Minimum turn-on resistance dependence on V-groove depth

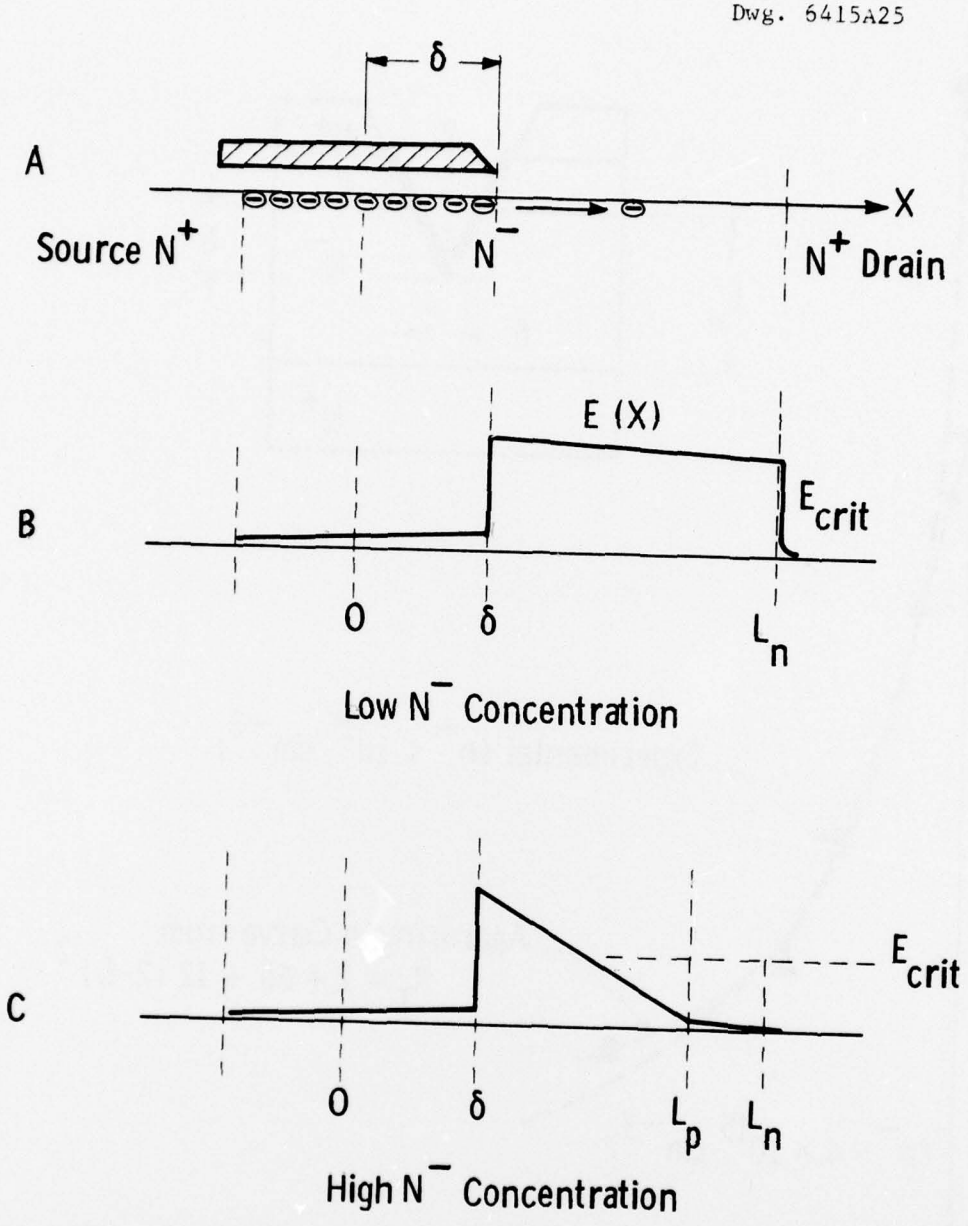


Fig. 5.4 — Field distributions for low and high N^- concentrations

Since $R_{SC} \propto (L_n - \delta)$, the obvious solutions to minimize this effect are to reduce L_n or increase δ. Both solutions, however, are at the expense of breakdown voltage and increased gate-drain capacitance. A better solution to this problem is to increase the n^- concentration, so that at low drain voltages the n^- region is not completely punched-through, as shown in Figure 5.4c. For an n^- concentration of 3×10^{15} cm^{-3}, for example, L_p is only 0.9 μm. This reduces R_{SC} by almost a factor of 5, as seen earlier in Section 4.1.2 and in Figure 5.3. The undepleted $(L_n - L_p)$ region, however, will give rise to another drain resistance component which can be minimized by allowing the $n^- - n^+$ interface to be slightly graded, as shown in Figure 4.5 earlier. This solution also has another unwanted effect, in that the output drain capacitance is now voltage dependent at low voltages. Consequently, the linearity of the device is expected to deteriorate, and some compromise solution between power and linearity has to be established during the design stage.

5.4 VMOST Breakdown Voltage

The concentration of the n^- region also appears to have an effect on the breakdown capability of VMOST devices with the top-source geometry, as shown in Figure 5.5. For low n^- concentrations there are two distinct regions of breakdown behavior characterized by the width of the n^- region. In region I, V_{B1} is independent of L_n and the mechanism for breakdown may be attributed to electron-hole multiplication and hole injection into the p-base region resulting in a "snap-back" type current-voltage breakdown characteristic.[2]

Breakdown in region II is attributed to normal avalanche breakdown in the drain region when the field has exceeded the ionization field. Because of this, V_{B2} is dependent directly on L_n.

By increasing the n^- concentration to $\sim 4 \times 10^{15}$ cm^{-3}, the breakdown voltage was seen to increase by almost a factor of 2. A

---

(2) Kennedy et al., IEDM Proceedings, 1974.

Curve 656011-A

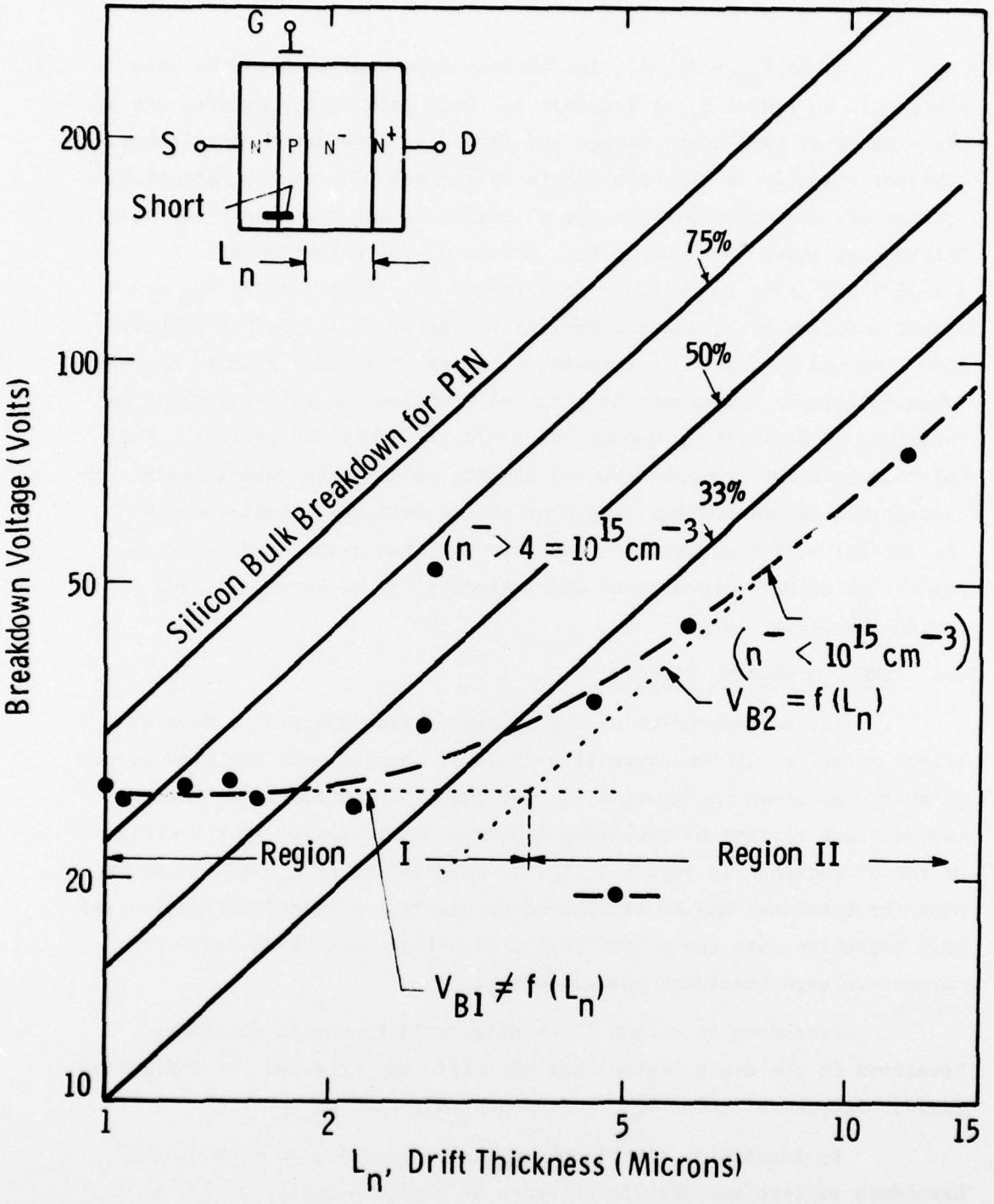


Fig. 5.5 – VMOST breakdown voltage characteristic (top - source geometry)

quantitative model for this behavior has not been developed, and should constitute one of the basis for future development work.

6. CONCLUSION

During this period two new VMOST geometries, Mark VI and Mark VII, were designed and studied with, unfortunately, limited success. The work planned was more ambitious than had originally been envisaged, due primarily to problems of evaluation, oxide contamination, and device design. These problems, however, were unexpected and much effort was expended in modelling and understanding the various observed behaviors. The results provided considerable insights into oxide contamination arising from KOH etching, and the dependence of turn-on resistance on gate-drain metal overlap and n^- concentration.

Further improvements in device power performance were also achieved with refinements in low angle evaporation of top-source VMOST devices. The marked increase in breakdown voltage obtained with higher n^- concentration devices has allowed the achievement of up to 10W of output power with high gain at 1 GHz.

The frequency-power capabilities of VMOST devices developed during the course of this program have still not been exceeded by any other silicon MOST devices. To achieve these levels of performance required a systematic optimization of the various device parameters. as characterized by Table 6.1. The input, feedback, and output capacitances, for example, are far superior to other devices and are a reflection of what has to be achieved in order to obtain high frequency performance.

Of the three basic top-source types of VMOST devices which were developed to completion, the high-angle (78°) transistor gave the highest frequency performance (f_{max} > 4 GHz). The highest power output was achieved with the low angle (60°) device, and the lowest parasitic capacitances with the V-groove VMOST (Table 6.1). The salient points of each device are shown in Table 6.2. In short, depending on the application and frequency requirements, a different design may be necessary.

DEVICE	Gate Length (L_g, μm)	Gate Width (W, cm)	g_m/W (μmho/μm)	Input		Feedback	Output
				C_{gc}/W (FF/μm) Gate-Channel	C_{gp}/W (FF/μm) Gate-Source Overlap	C_{gd}/W (FF/μm)	C_{ds}/W (FF/μm)
(W) Angle Evaporated VMOST (78°)	1 - 1.5	1.72	14 - 15	0.3 - 0.4	0.4	0.12 - 0.17	0.3 depending on n^- width
(W) V-Groove VMOST	1.5	1.1	8 - 9	0.4	0.16	0.11	0.26 (n^- = 2μm)
Siliconix V-Groove	>2	2.54	11	← 1.9	(Total) →	0.28	1.37

TABLE 6.1 Vertical Channel MOST Parameters

TABLE 6.2 Comparison of VMOST Devices

Device	Advantages	Disadvantages
High-angle Isotropic-etch VMOST (e.g., Mark V)	High frequency capability High geometric gate reduction Isolation of parasitic gates Clean fabrication process High transconductance Low turn-on resistance Moderate yield	Tight fabrication control Multi-metal system Gate-metal spread High input capacitance Metal etching to minimize source resistance
Low-angle Isotropic-etch VMOST (e.g., modified Top-source Mk VI)	Improved gate definition Single metal system Low geometric gate reduction Clean fabrication process High transconductance High yield	Inefficient parasitic gate isolation Deeper n^+ source diffusion required
Zero-angle Anisotropic-etch V-groove VMOST (e.g., Mark VII)	High gate periphery/area Self limiting etching 0° metal evaporation Single metal system Rigid oxide overhang Low parasitic capacitances	Crystallographic alignment required Inefficient parasitic gate isolation No geometric gate reduction K contamination possibility Lower transconductance Deeper n^+ source diffusion required

7. RECOMMENDATIONS FOR FUTURE WORK

Even at the conclusion of this program a number of improvements in device design can still be made, some of which are obvious, e.g., minimization of slit width dimensions from present 3-4 μm design rules to below 2 μm; optimization of n^- concentration and width; and the introduction of differential oxide growths in V-groove devices. Furthermore, the problem of profile evaluation in back-filled epitaxy for Mark VI VMOST designs remains yet unsolved.

Two main areas of research and development appear to be the most fruitful for future work. The first is the size of the VMOST device that can be practically realized with good yield. Devices with 3 to 5 times the present gate periphery (1.7 cm) appear to be feasible with today's technology, to yield up to 10A of drain current and transconductances approaching 1 mho. A single transistor cell of this kind will have a peak dc power capability of nearly 500W, and should be capable of delivering up to 50W at 1 GHz.

Another area of interest is the study of breakdown behavior in various vertical channel MOS transistor designs as related to their power and frequency performance. Much of this area remains untouched today.

Contract N00014-74-C-0012

Distribution List

Office of Naval Research
Arlington, Virginia 22217
Attn: Code 427 (4)

Hewlett-Packard
1501 Page Mill Road
Palo Alto, California 94304
Attn: Dr. R. Archer (1)

Hughes Research Laboratories
Malibu Canyon Road
Malibu, California 90265
Attn: M. Waldnew (1)

Raytheon Company
28 Seyon Street
Waltham, Massachusetts
Attn: R. Behrig (1)

RCA Laboratories
David Sarnoff Research Center
Princeton, New Jersey 08540
Attn: M. Nowogrodzki (1)

Texas Instruments
Mail Stop 118
P.O. Box 5012
Dallas, Texas
Attn: J. Pankratz/M. Macksey (1)

Naval Air Systems Command
Washington, D.C. 20360
Attn: (AIR-360) (1)

Varian Associates
Corporate Solid State Lab.
611 Hansen Way
Palo Alto, California 94303
Attn: Dr. R. Bell (1)

Naval Research Laboratory
4555 Overlook Avenue, S.W.
Washington, D.C. 20375
Attn: Code 5211 (1)
5250 (1)

DCASR (1)
P.O. Box 7478
Philadelphia, PA 19101

Defense Documentation Center (12)
Bldg. 5
Cameron Station
Alexandria, Virginia 22314

AGED (1)
201 Varick Street
9th Floor
New York, New York 10014

Commanding General (1)
U.S. Army Electronics Command
AMSEL-TL-IC
Ft. Monmouth, N.J. 07103

New York Area Office (1)
Office of Naval Research
715 Broadway, 5th Floor
New York, New York 10003

Siliconix, Inc.
2201 Laurelwood Road
Santa Clara, California 95054
Attn: E. Oxner (1)

F. Ressler (1)
Naval Air Development Center
Warminster, PA 18974